

# 648-M7

## 648FX-M7

## 661FX-M7


Rev: 3.0


### Revision History :

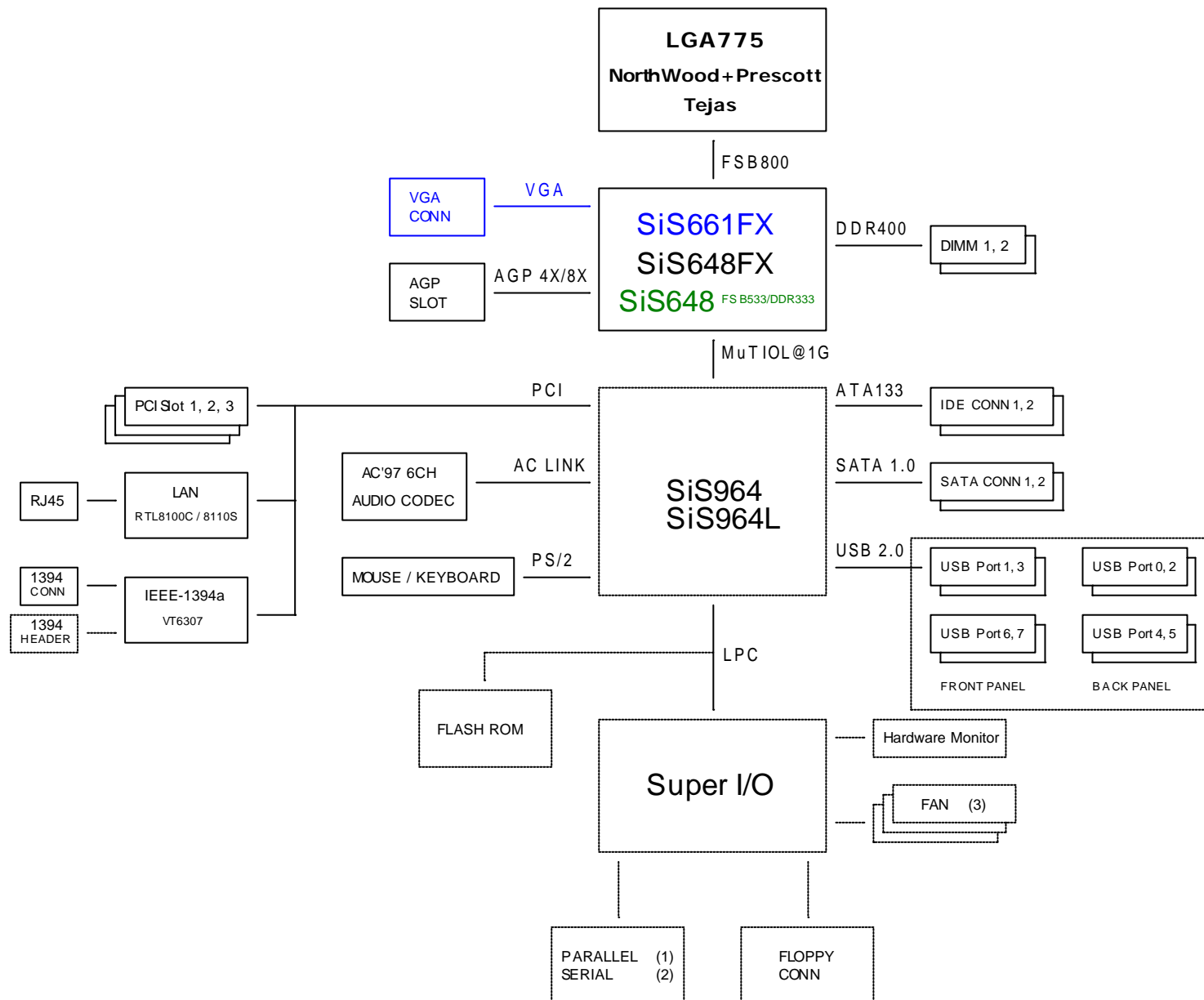
1. Ver A: Initial for 661FX/648FX for LGA775
2. Ver 1.0:
  - I. modify CPU pull-high
  - II. add FSB1066 select CKTs
  - III. modify Common-Choke and R0603 co-lay
  - IV. add 1394A3 header
  - V. AD1888 and ALC655 co-lay
  - VI. modify FAN CTRL CKTs
  - VII. modify VRDGD
  - VIII. add PANEL2
3. Ver 1.1:
  - I. modify for EE CPU supporting
  - II. modify SmartFAN clamp up circuit
4. Ver 1.1A:
  - I. modify for CPU 3pin SmartFAN supporting
  - II. Add SLVU2.8-4 Surge Protect IC
5. Ver 1.2:
  - I. move CPU socket location
6. Ver 3.0:
  - I. add CNR solt
  - II. remove AD1888 co-lay

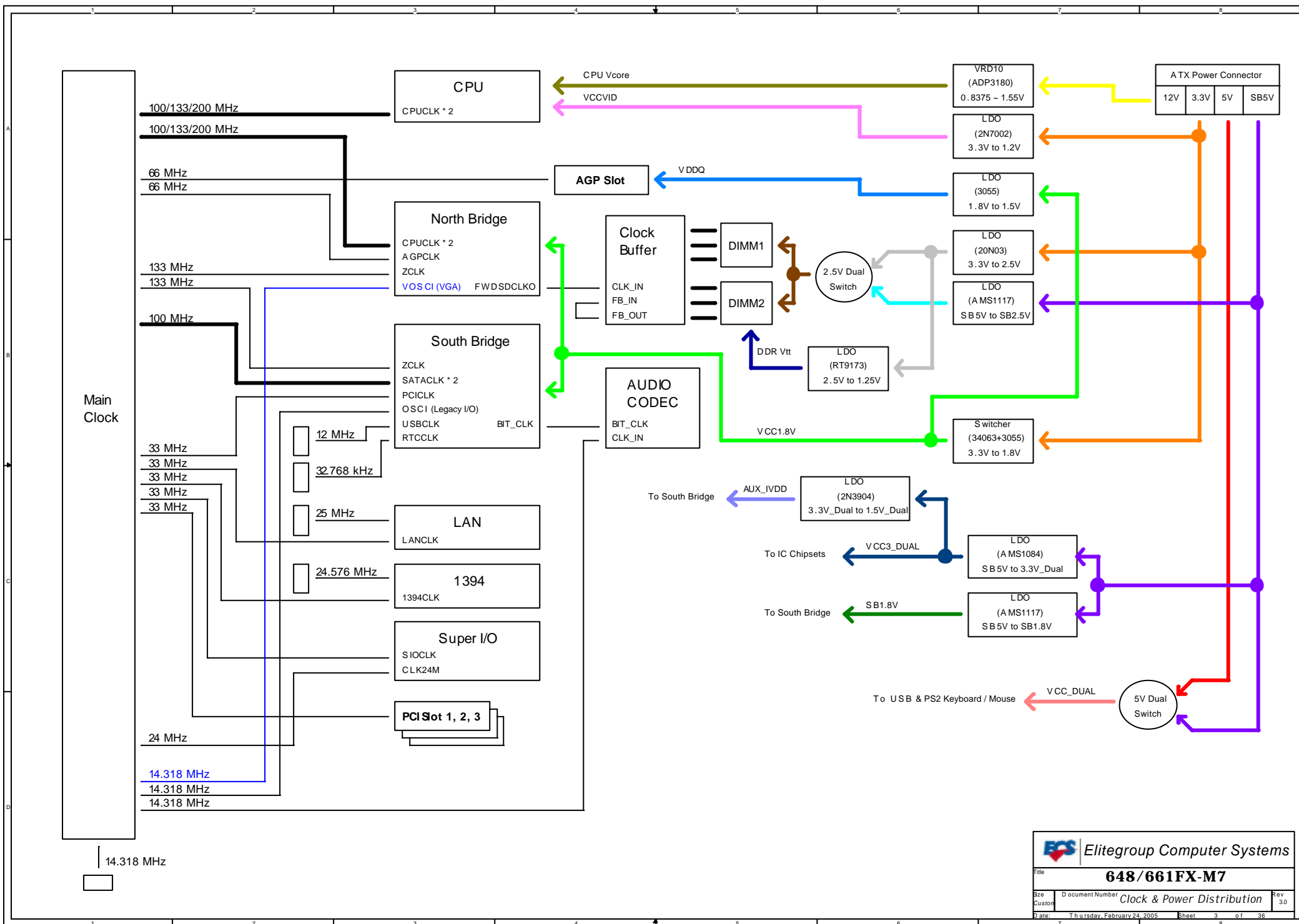
### Page Index =====

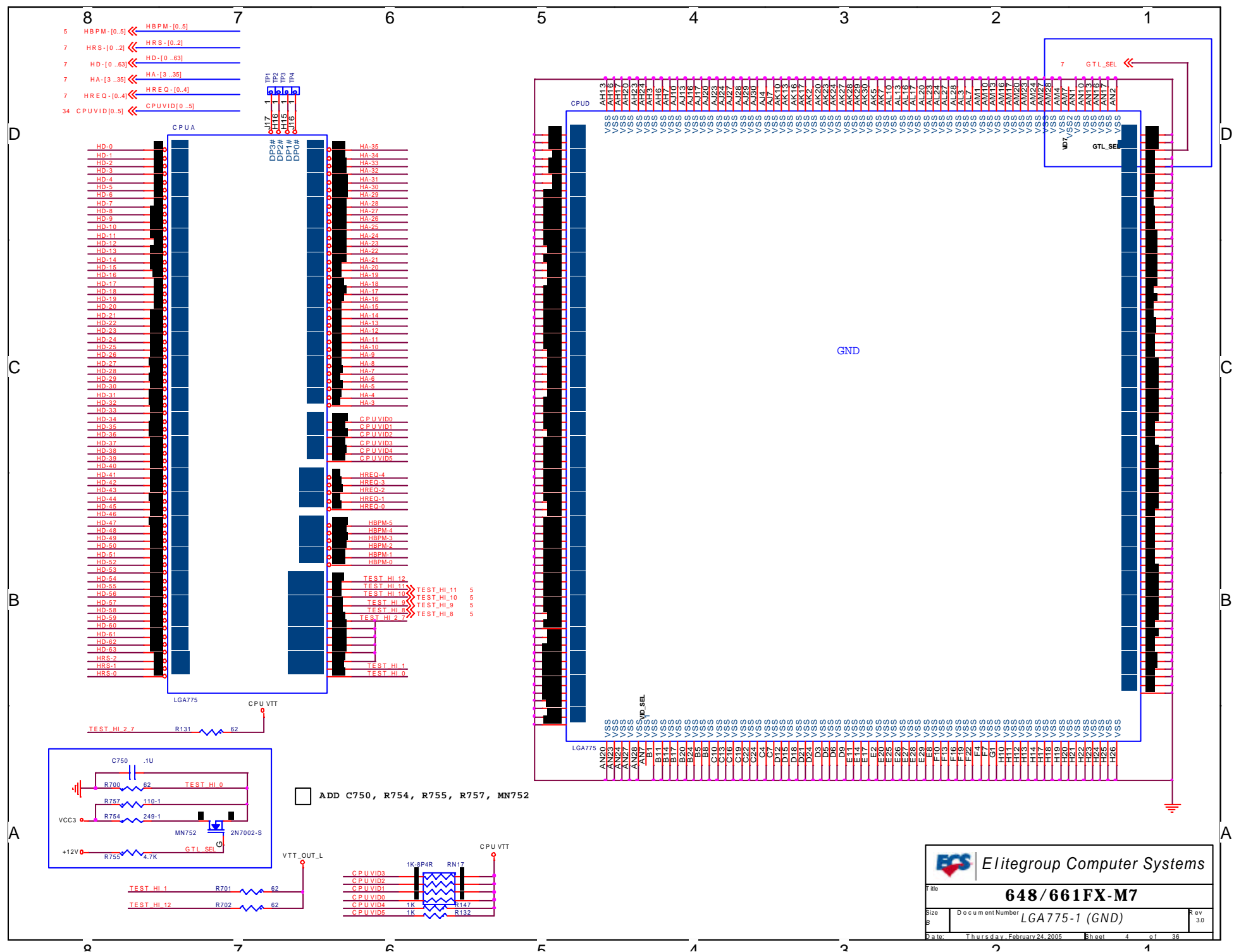
- |                                     |                               |
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| 5. Socket LGA775-2                  | 25. IEEE1394a                 |
| 6. Socket LGA775-3                  | 26. Audio Codec               |
| 7. SiS661FX-1 (HOST / AGP)          | 27. Audio Interface           |
| 8. SiS661FX-2 (Memory)              | 28. Super I/O                 |
| 9. SiS661FX-3 (VGA / HyperZip)      | 29. KB/MS/ROM/FDC/IR          |
| 10. SiS661FX-4 (Power)              | 30. COM 1,2 / LPT             |
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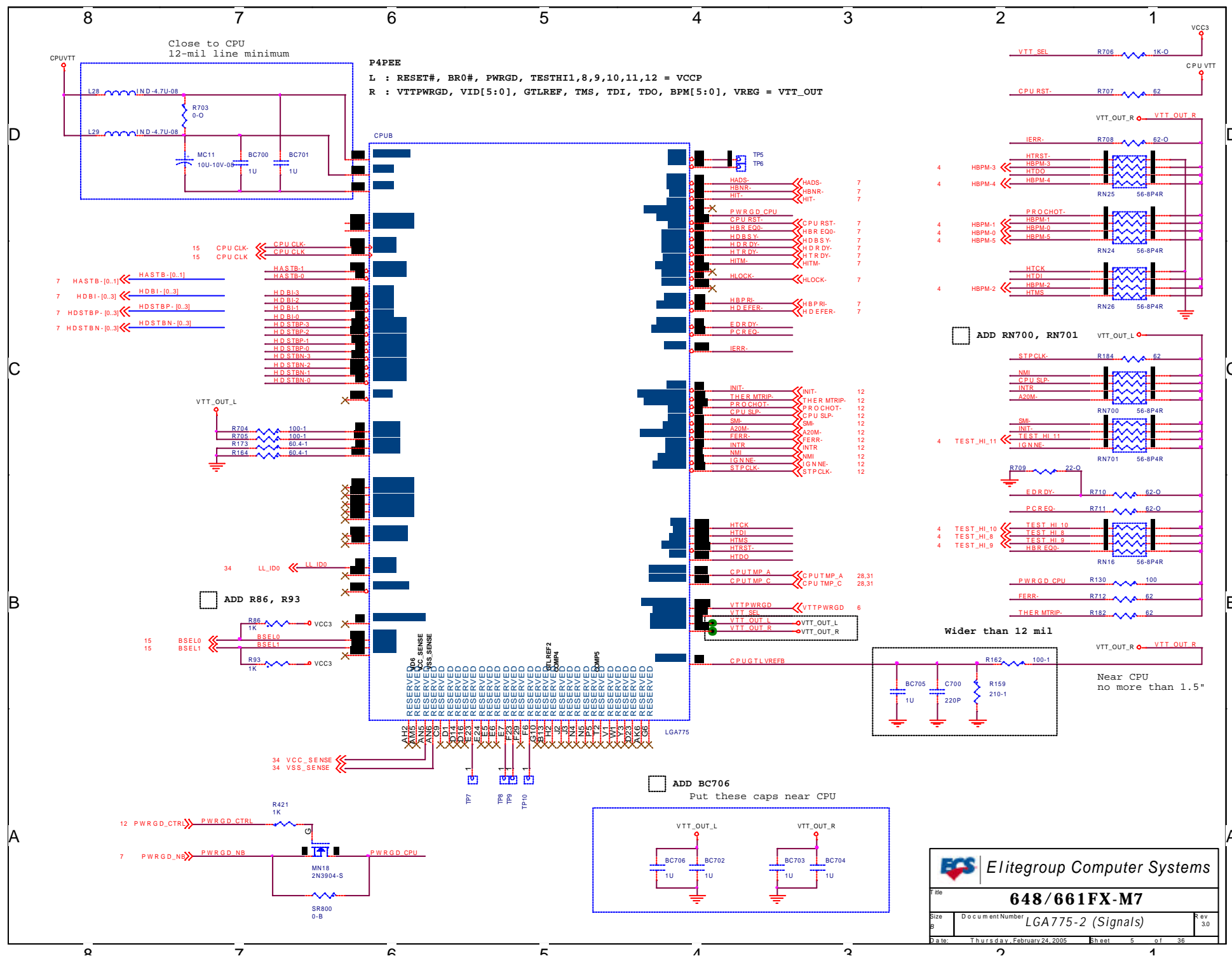
	<b>SIGNATURE</b>	<b>DATE</b>
<b>DESIGNER</b>	LukeLin	
<b>LAYOUT</b>	ECS Layout team	
<b>CHECK</b>	LukeLin	
<b>APPROVAL</b>		

 Elitegroup Computer Systems	
Title <b>648/661FX-M7</b>	
Customer <b>Cover Sheet</b>	3.0
Date: Thursday, February 24, 2005 Sheet 1 of 36	



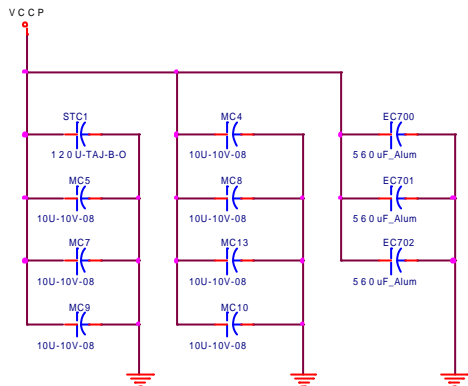




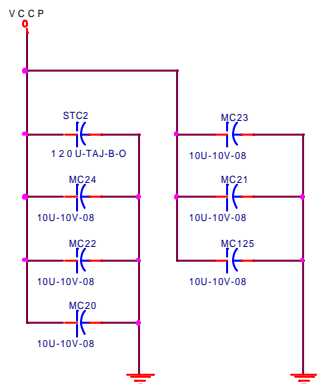


P.S. Choose XSR components instead of Y5V for all 22uP\_1206 capacitors on this page.

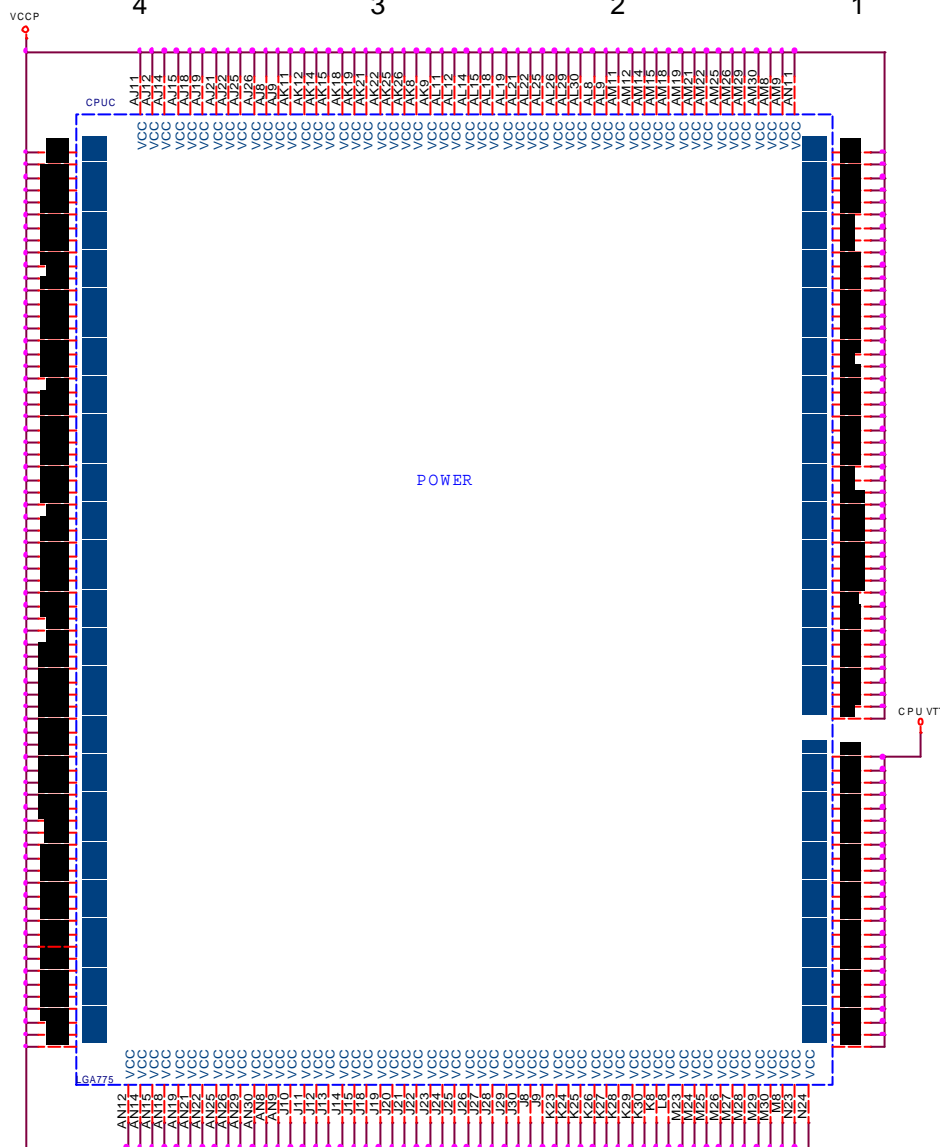
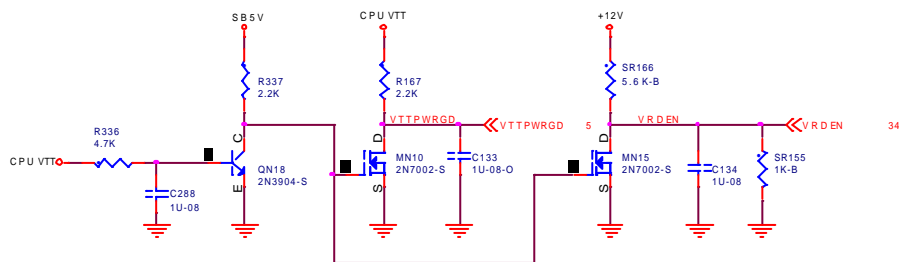
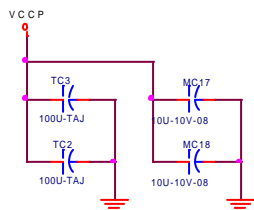
Put these capacitors at processor TOP SIDE

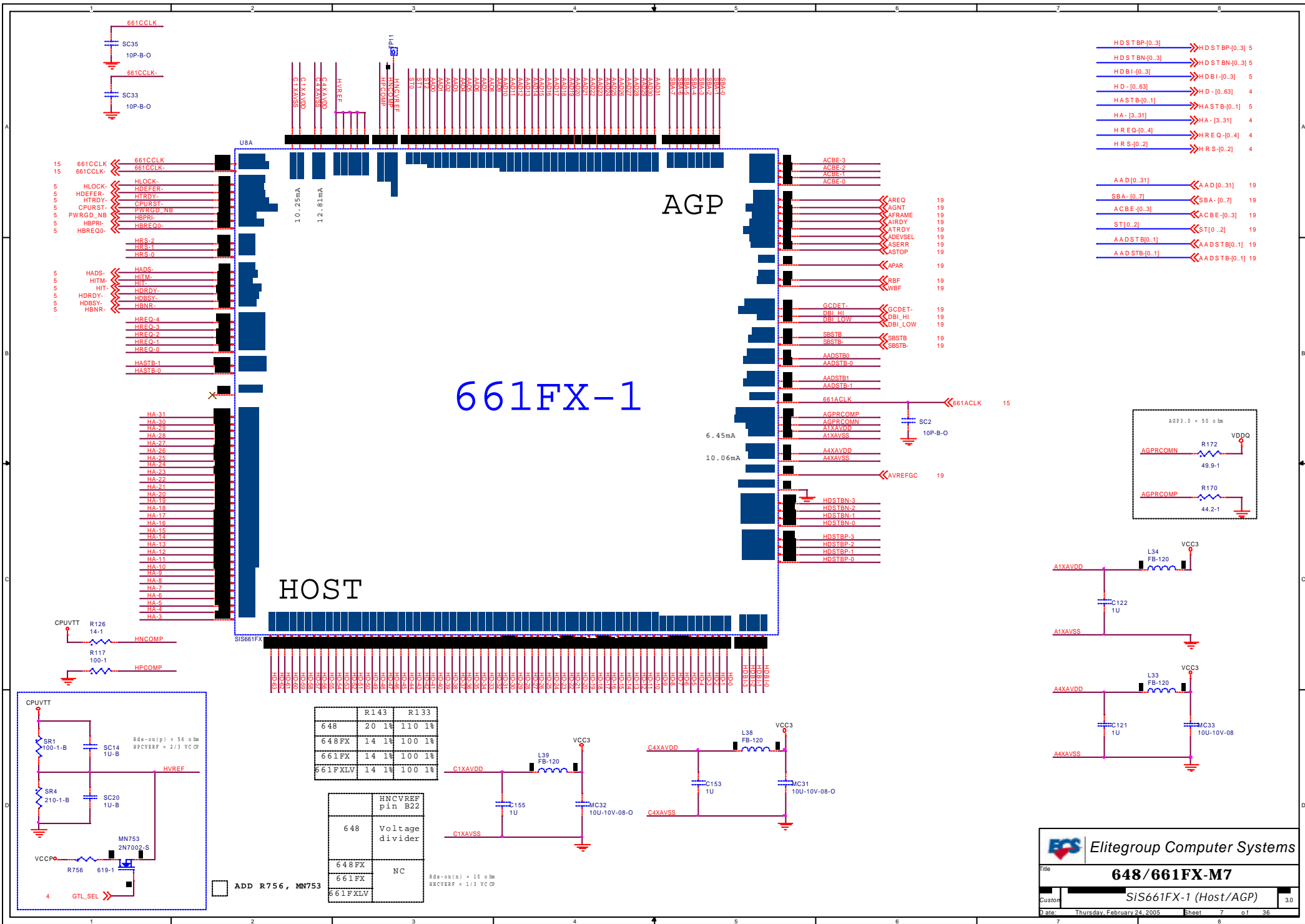


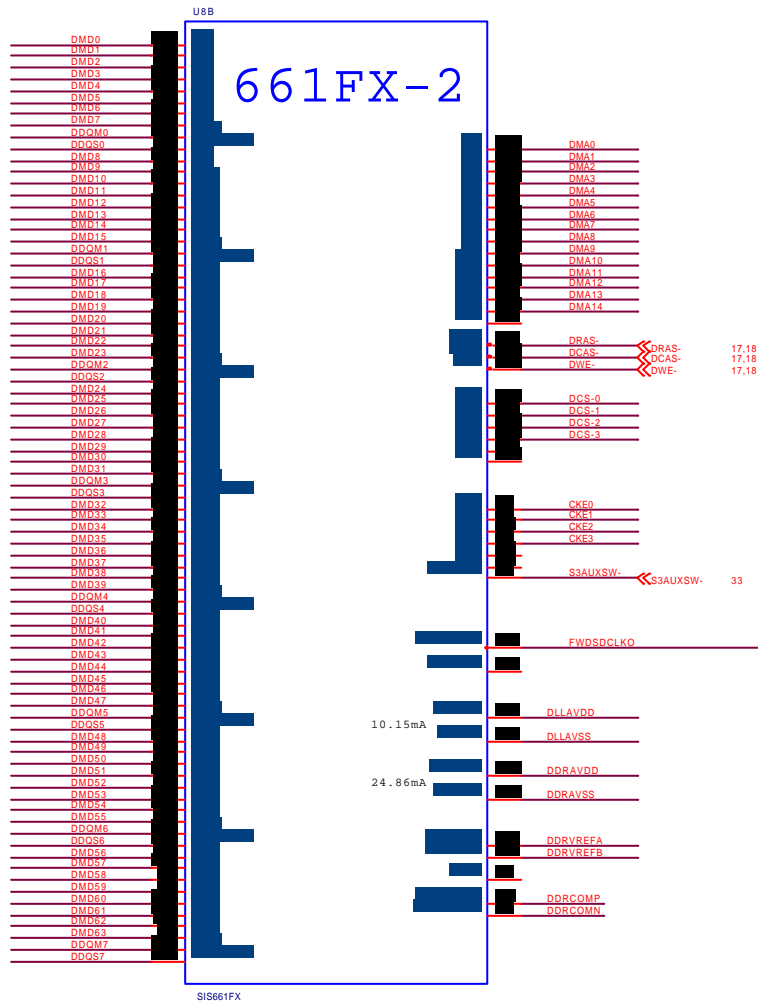
Put these capacitors at processor LEFT SIDE



Put these capacitors INSIDE PROCESSOR CAVITY











661FX-4

Power

NOTE:  
SiS 648FX doesn't have  
the following 9 balls  
VDDQ(P12), VDD(AE14), VDDM(AE15),  
VDDM(AB25), IVDD(N20), IVDD(T24),  
VTT(M20), VTT(N25), VTT(P25).

AU X\_IVDD=10.12mA  
AU X3.3=26.38mA

253.65mA

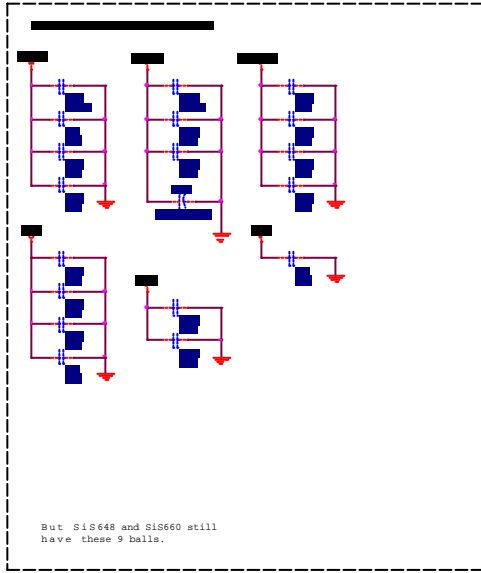
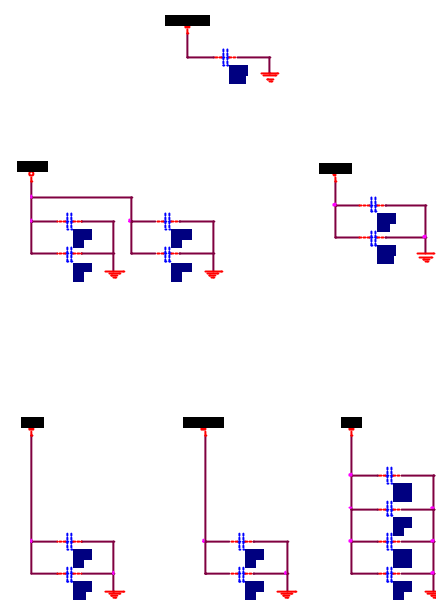
IVDD for VGA 104mA  
IVDD 1310mA

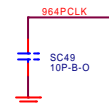
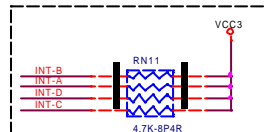
111mA

26

488.91mA

239.09mA





22,23,24,25 CBE- [0..3] << CBE- [0..3]

9,19,22,23 INT-A  
19,22,23,25 INT-B  
22,23,24 INT-C  
22,23 INT-D

22,23,24,25 FRAME-  
22,23,24,25 IRDY-  
22,23,24,25 TRDY-  
22,23,24,25 STOP-

22,23,24 SERR-  
22,23,24,25 PAR-  
22,23,24,25 DEVSEL-  
22,23 PLOCK-

15 964CLK  
19,20,22,23,24,25,29 PCIRST-  
28 SIO PCIRST-  
9 NBPCIRST-

964CLK  
PCIRST-  
R209 33  
R210 33

964ZCLK 10P-Q

15 964ZCLK  
9 ZSTB0  
9 ZSTB-0

9 ZSTB1  
9 ZSTB-1

9 ZUREQ  
9 ZDREQ

SZCMP\_N

SZCMP\_P

SZ1XAVDD

SZ1XAVSS

SZ4XAVDD

SZ4XAVSS

SZVREF

ZAD16

9 ZAD [0..16] <<

22,23,24,25 AD[0..31] << AD[0..31]

PCI

IDE

964-1

HyperZip

1.0mA

U13A

ICH RDYA << ICHRDYA 20  
IDEREQA << IDEREQA 20  
ID EIRQA << ID EIRQA 20  
CBLIDA << CBLIDA 20

ID EIOR-A << IDEIOR-A 20  
ID EIQW-A << IDEIQW-A 20  
ID EACK-A << IDEACK-A 20

ID ESAA2 << ID ESAA2 20  
ID ESAA1 << ID ESAA1 20  
ID ESAA0 << ID ESAA0 20

ID ECS-A1 << IDECS-A1 20  
ID ECS-A0 << IDECS-A0 20

ICH RDYB << ICHRDYB 20  
IDEREQB << IDEREQB 20  
ID EIRQB << ID EIRQB 20  
CBLIDB << CBLIDB 20

ID EIOR-B << IDEIOR-B 20  
ID EIQW-B << IDEIQW-B 20  
ID EACK-B << IDEACK-B 20

ID ESAB2 << ID ESAB2 20  
ID ESAB1 << ID ESAB1 20  
ID ESAB0 << ID ESAB0 20

ID ECS-B1 << IDECS-B1 20  
ID ECS-B0 << IDECS-B0 20

IDEDA0  
IDEDA1  
IDEDA2  
IDEDA3  
IDEDA4  
IDEDA5  
IDEDA6  
IDEDA7  
IDEDA8  
IDEDA9  
IDEDA10  
IDEDA11  
IDEDA12  
IDEDA13  
IDEDA14  
IDEDA15

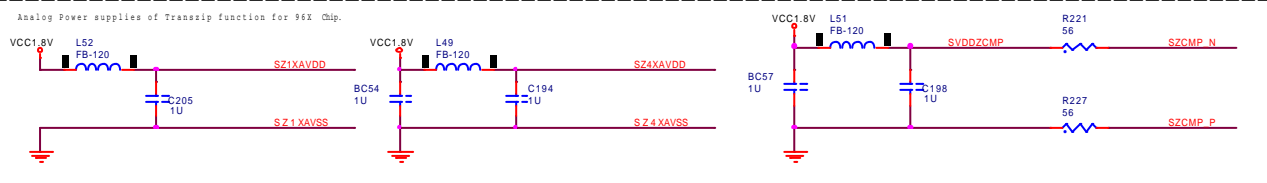
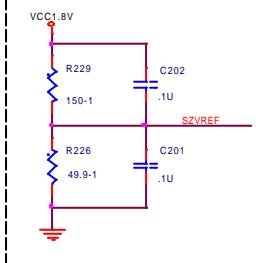
IDED A[0..15] 20

IDEDB0  
IDEDB1  
IDEDB2  
IDEDB3  
IDEDB4  
IDEDB5  
IDEDB6  
IDEDB7  
IDEDB8  
IDEDB9  
IDEDB10  
IDEDB11  
IDEDB12  
IDEDB13  
IDEDB14  
IDEDB15

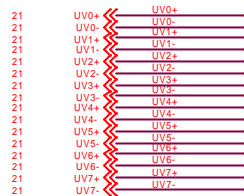
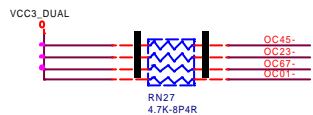
IDED B[0..15] 20

SIS964

ZAD0  
ZAD1  
ZAD2  
ZAD3  
ZAD4  
ZAD5  
ZAD6  
ZAD7  
ZAD8  
ZAD9  
ZAD10  
ZAD11  
ZAD12  
ZAD13  
ZAD14  
ZAD15





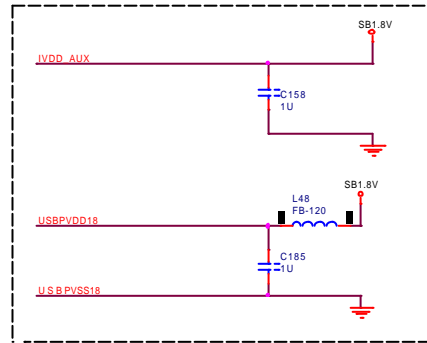
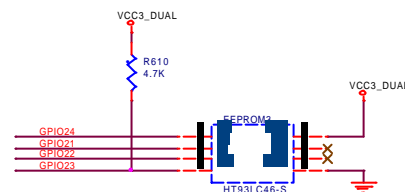
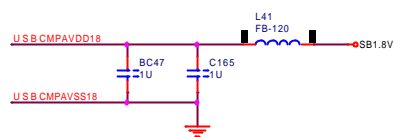
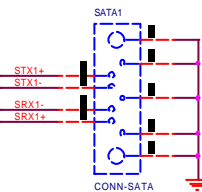
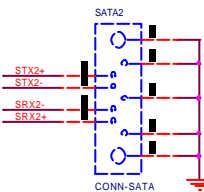
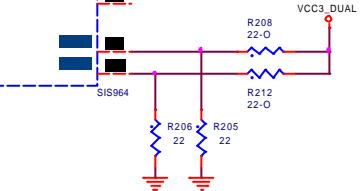
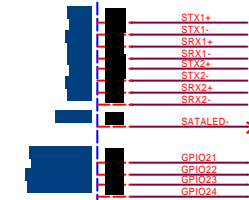
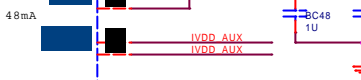
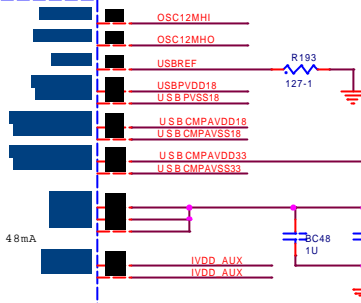
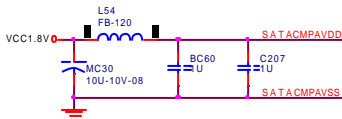
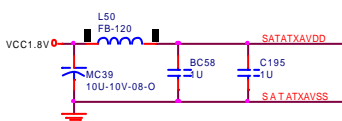
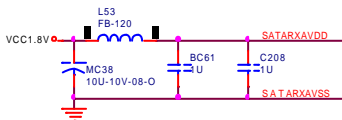
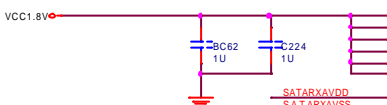
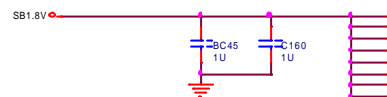


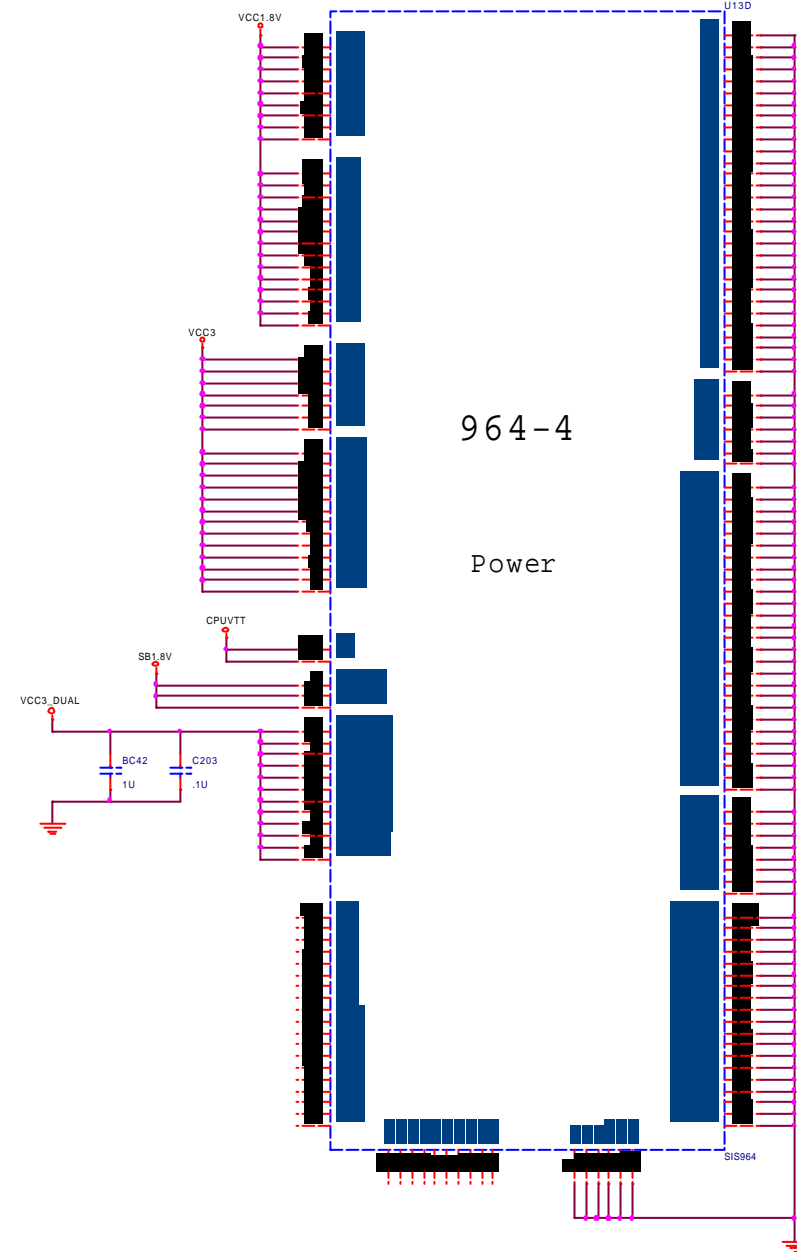
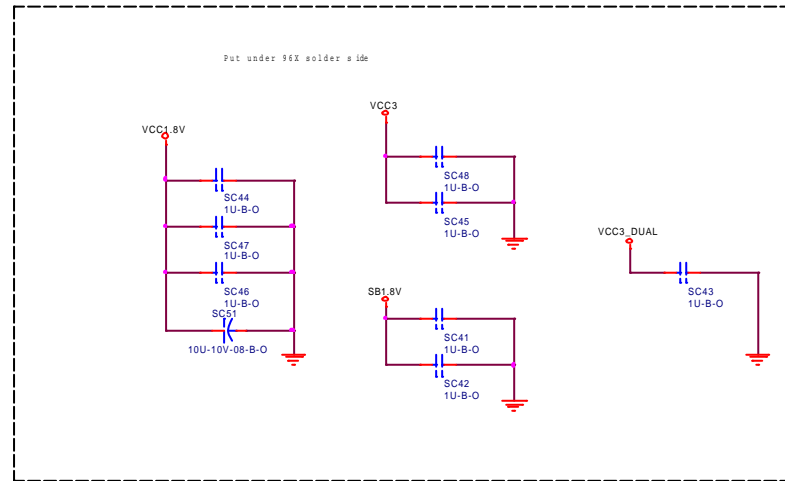
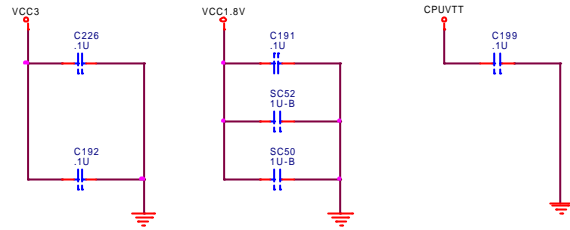
U13C

USB

330mA

964-3

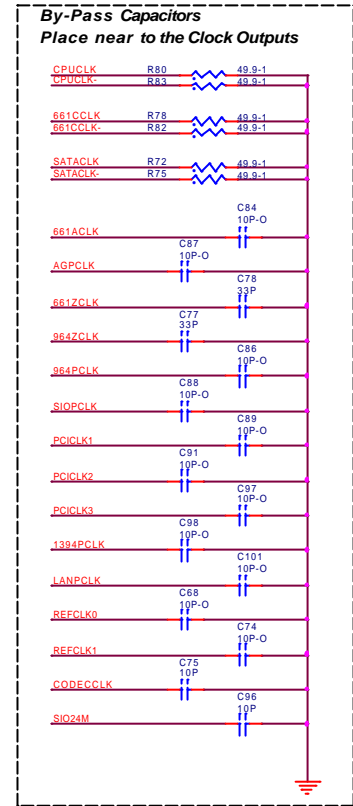
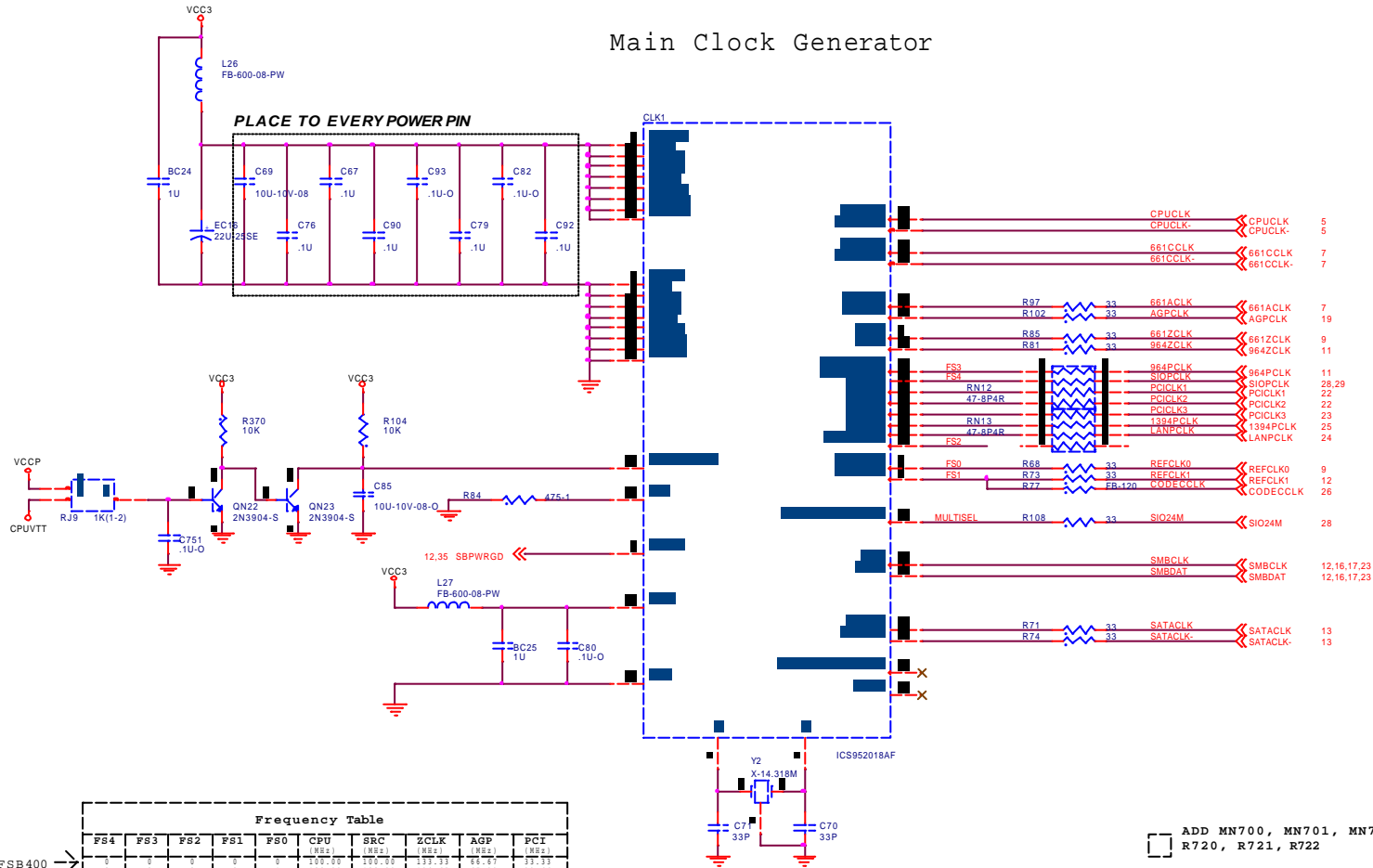




964-4

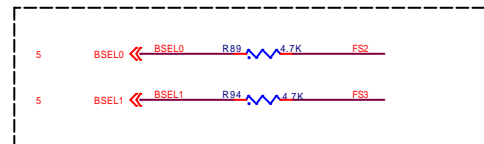
Power

# Main Clock Generator

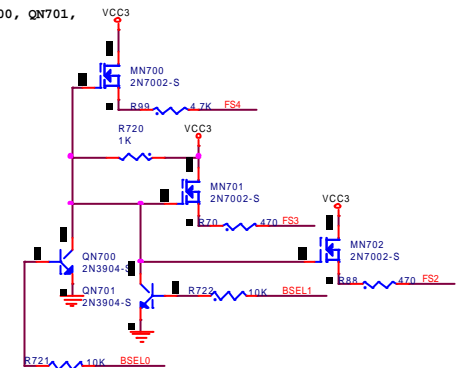


ADD MN700, MN701, MN702, QN700, QN701, R720, R721, R722

## Frequency Selection



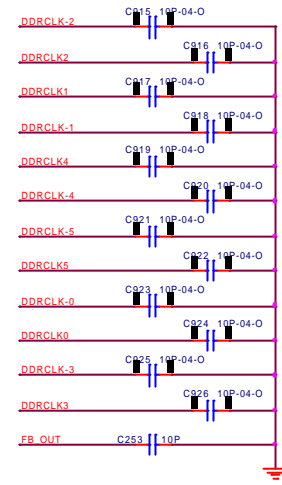
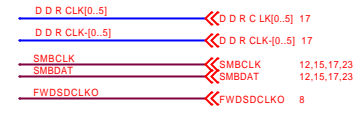
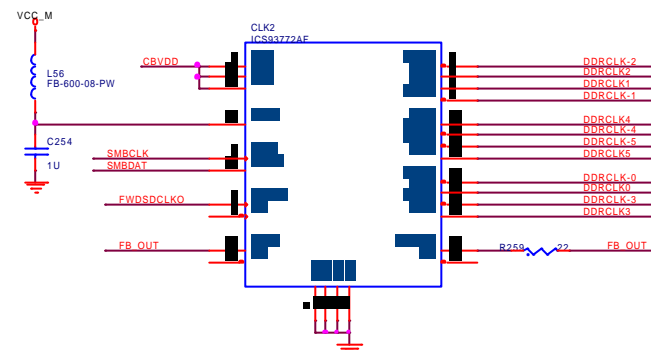
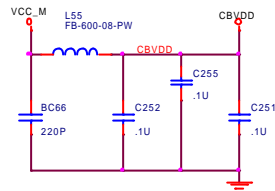
Clock Generator Table	FS4	FS3	FS2	FS1	FS0
Hardware Trapping	Low	Low	BSEL2	BSEL1	BSEL0
CPU=100 (BSEL[2:0]=101)					
CPU=133 (BSEL[2:0]=001)	0	0	1	0	0
CPU=166 (BSEL[2:0]=011)	0	1	1	0	0
CPU=200 (BSEL[2:0]=010)	0	1	0	0	0
CPU=266 (BSEL[2:0]=000)	1	1	1	0	0



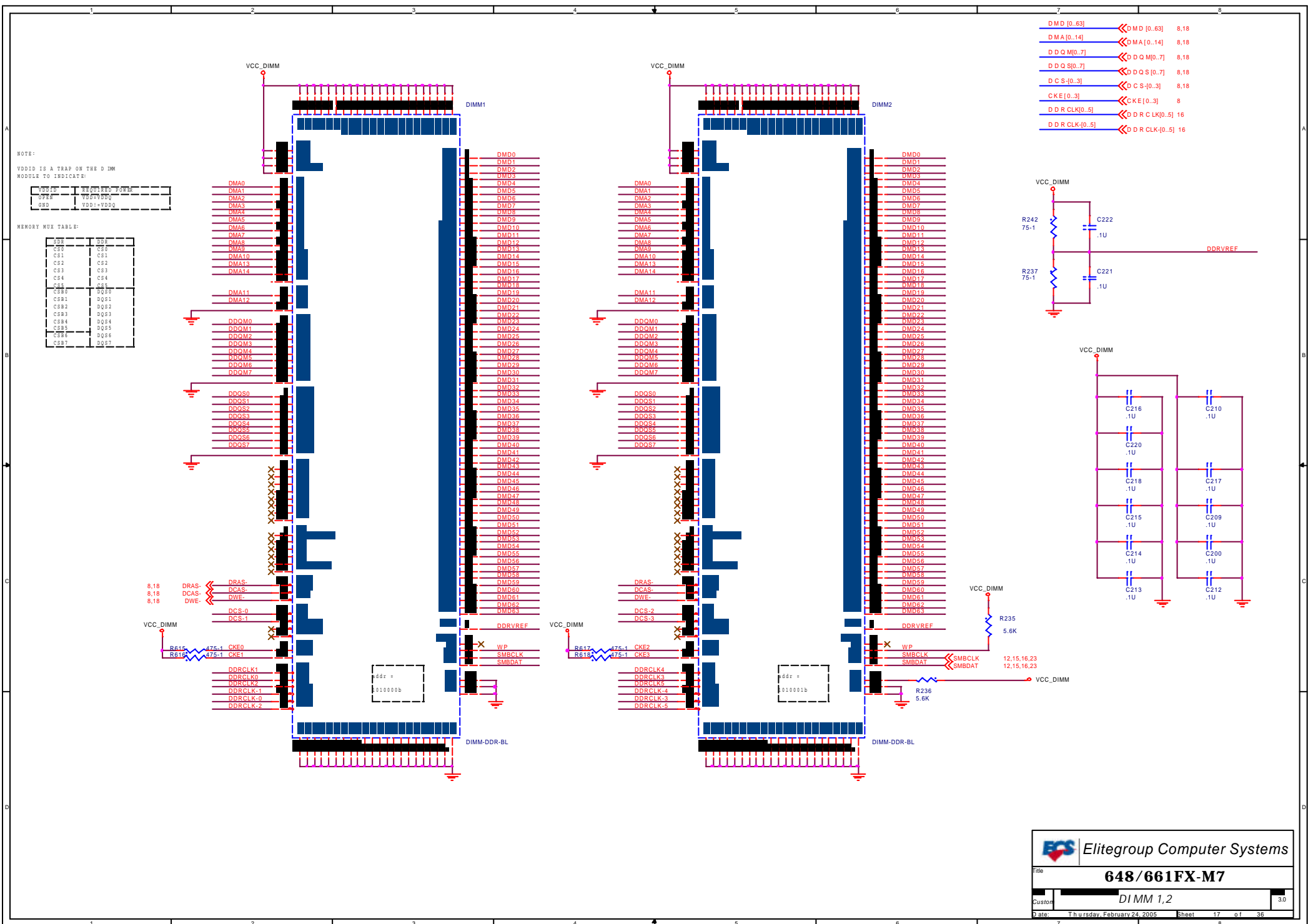
# Clock Buffer (DDR)

( 5 OPTIONS)  
 1: ( ICS ) ICS93716  
 2: ( Winbond )  
 3: ( ICWorks )  
 4: ( IMI )  
 5: ( AMI )

By-Pass Capacitors  
 Place near to the Clock Buffer



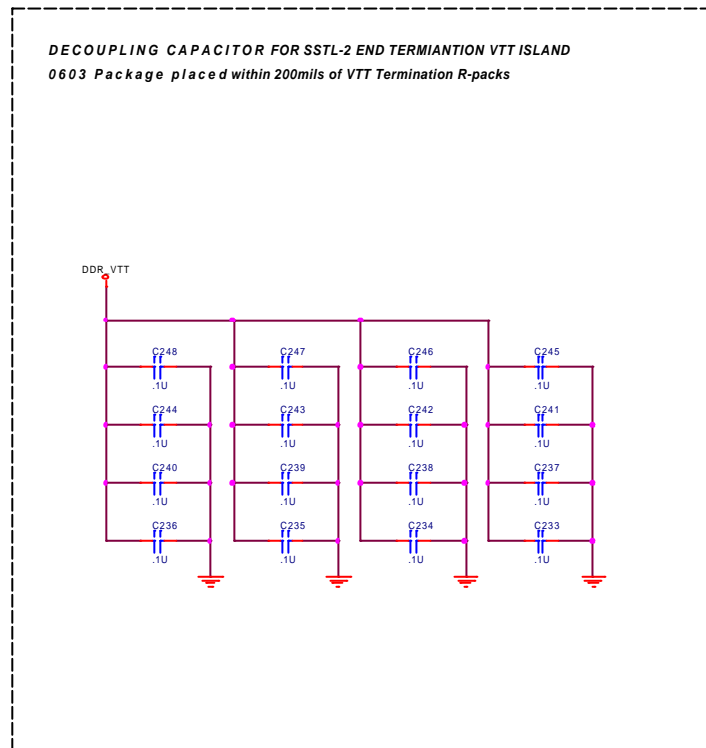
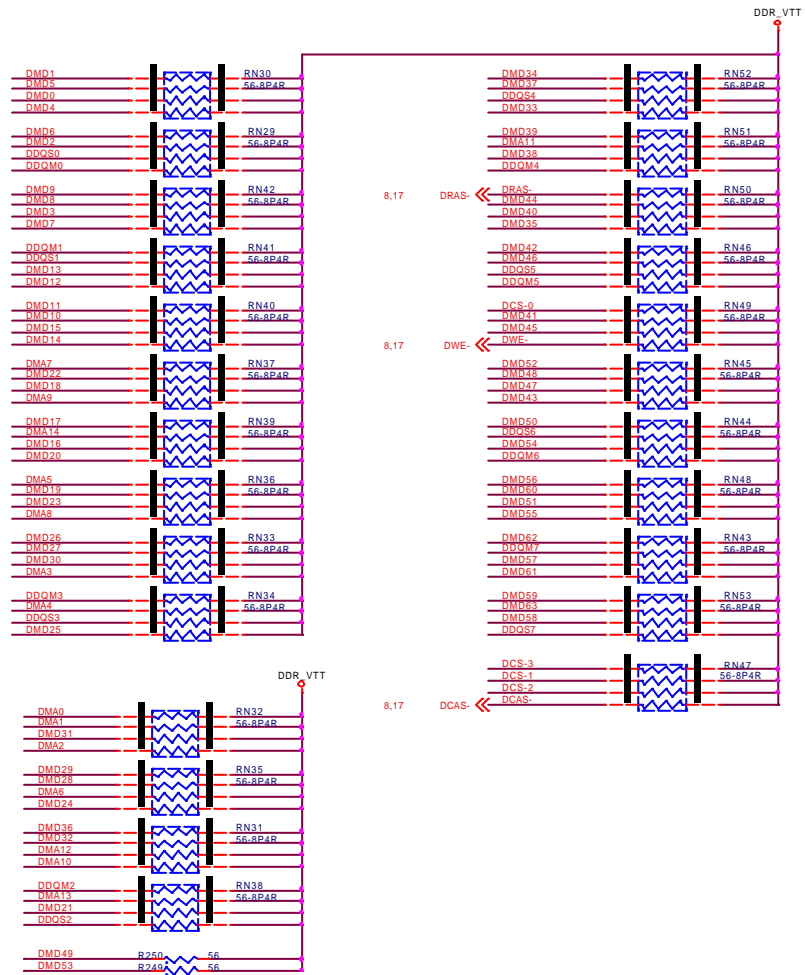




# SSTL-2 Termination Resistors

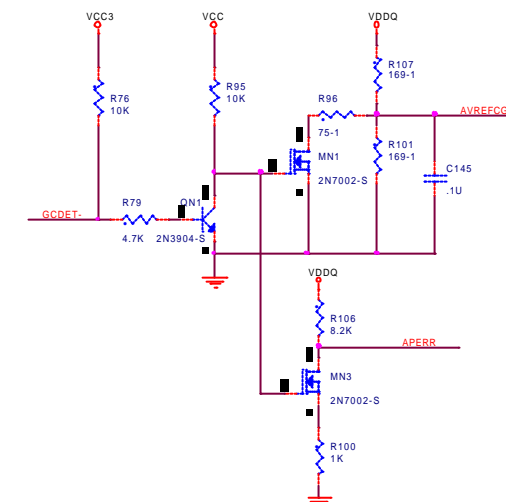
Signal	Termination	Value	Notes
Q/DQM (/DQS)	V-CMOS	10/-	SSTL-2
RA/Control	V-CMOS	0	SSTL-2
ES	V-CMOS	0	SSTL-2
TS	2.3.3V	0	2.5V

DMD [0..63]	8,17
DMA [0..14]	8,17
DDQM [0..7]	8,17
DDQS [0..7]	8,17
DCS [0..3]	8,17

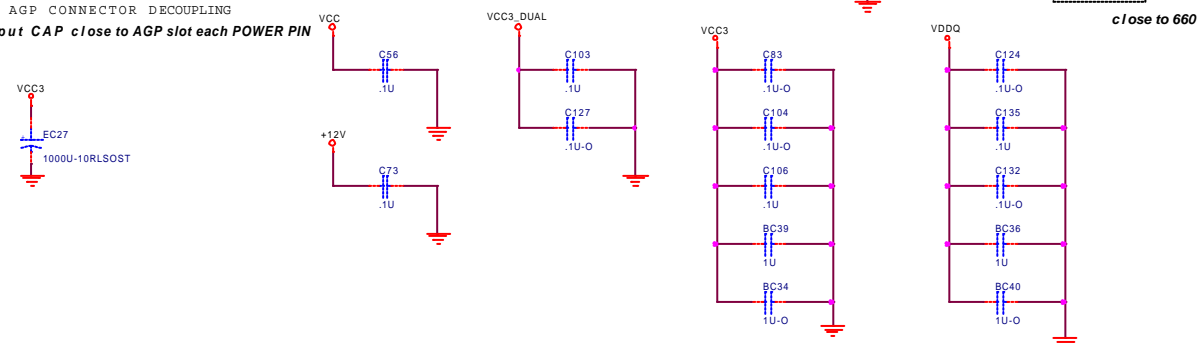


7	SBA-[0..7]	SBA-[0..7]
7	ST[0..2]	ST[0..2]
7	ACBE-[0..3]	ACBE-[0..3]
7	AAD[0..31]	AAD[0..31]
7	AADSTB[0..1]	AADSTB[0..1]
7	AADSTB[0..1]	AADSTB[0..1]

GCDET-	Low	Hi
Graphic Card	AGP 3.0	AGP 2.0
AVREFCG	0.35	0.75
APERR	0	1.5



AGP CONNECTOR DECOUPLING  
put CAP close to AGP slot each POWER PIN



Elitegroup Computer Systems

648/661FX-M7

AGP Slot

File

Size

Date:

Document Number

Thursday, February 24, 2005

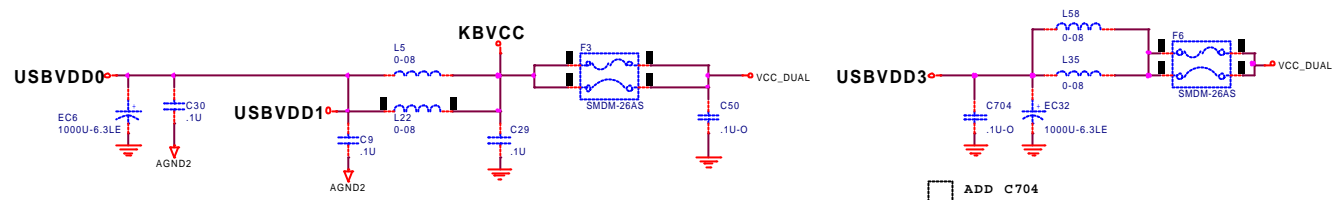
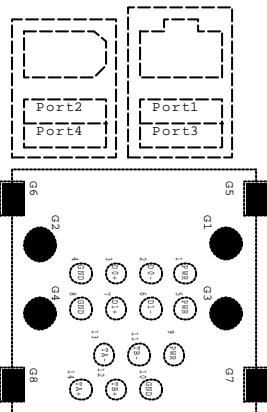
Rev

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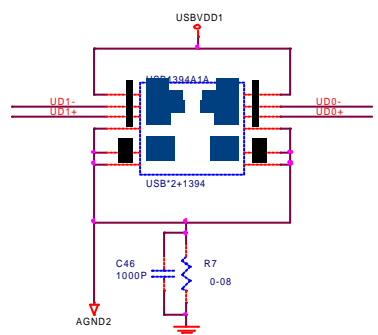
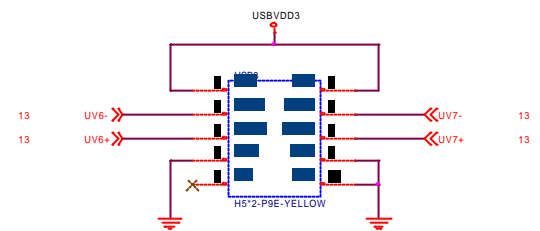
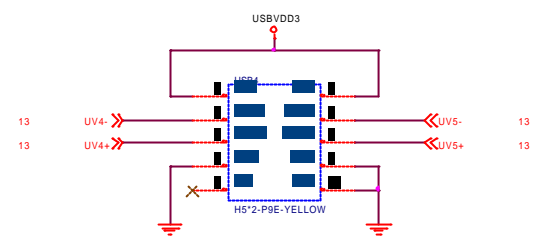
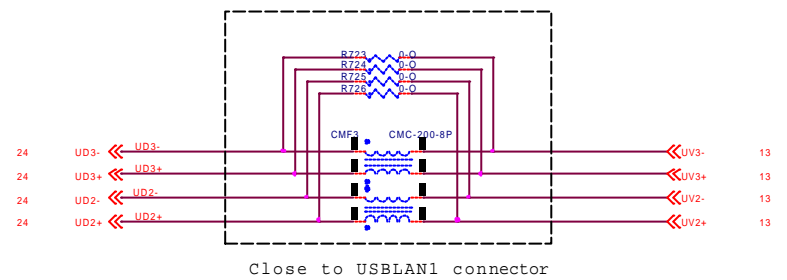
Sheet

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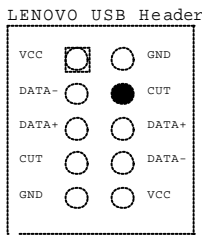
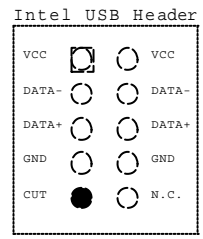
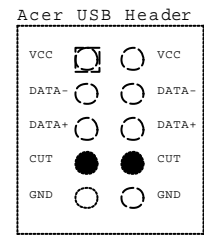
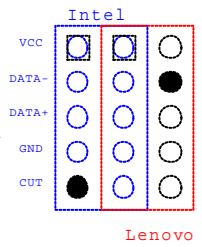
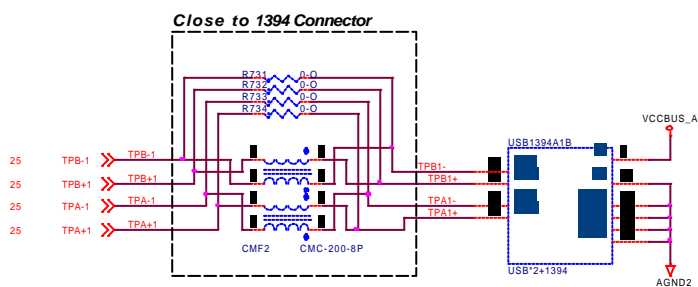
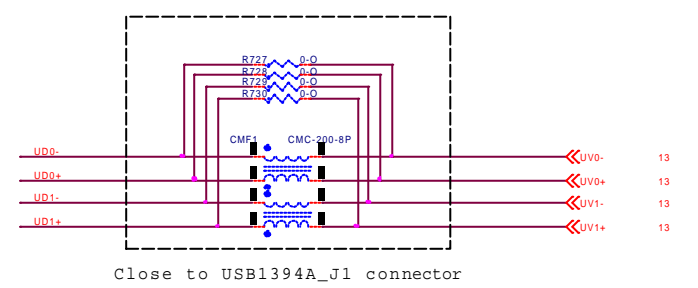


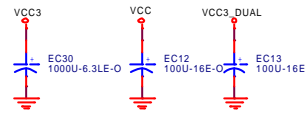


ADD C704



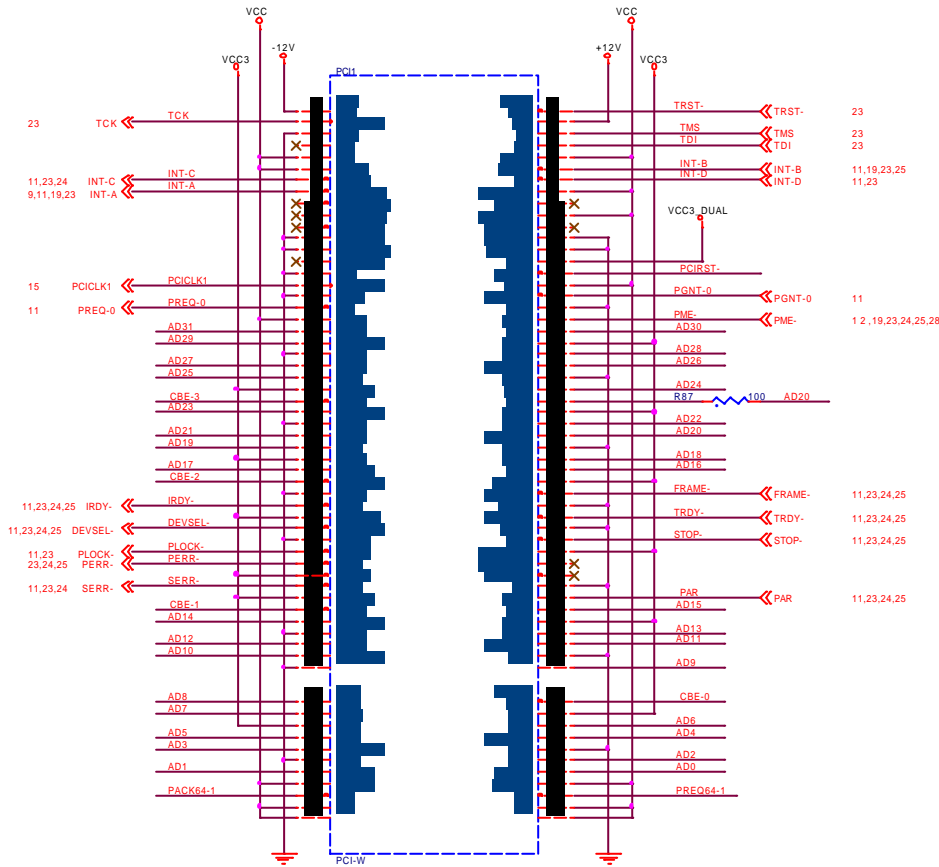
Control	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5



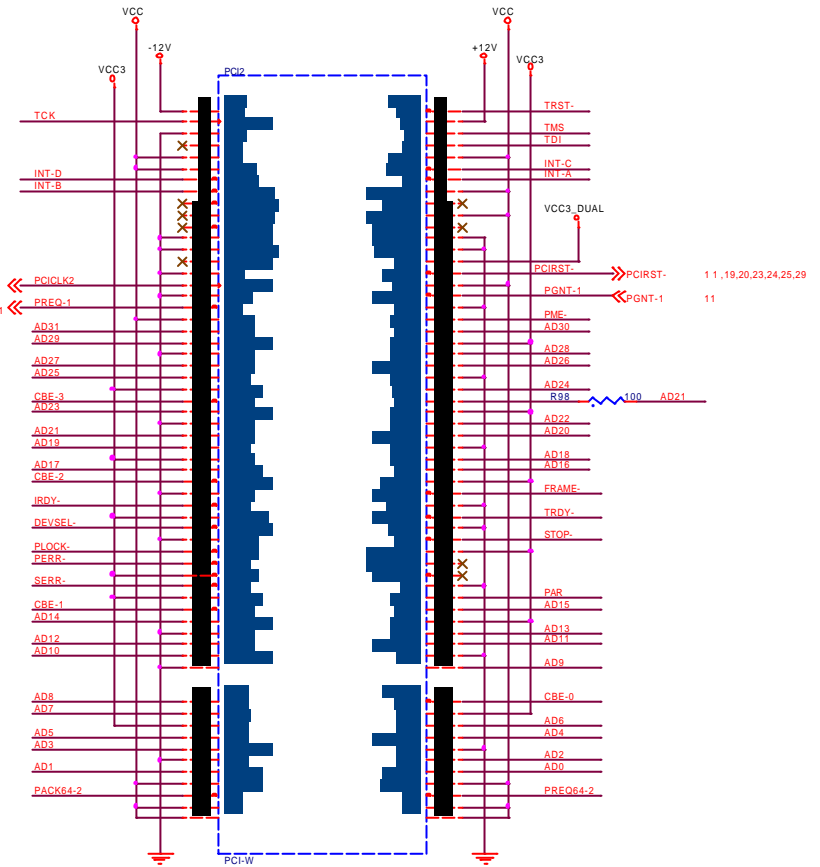


PCI Slot 1 & 2

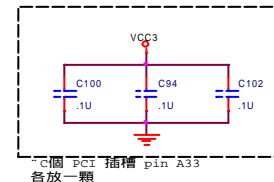
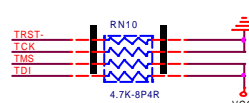
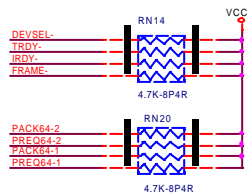
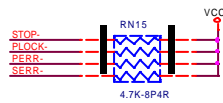
11,23,24,25 CBE-[0..3] AD[0..31]  
11,23,24,25 AD[0..31]



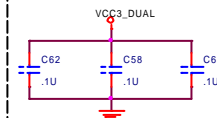
IDSEL=AD20  
INT[B,C,D,A]

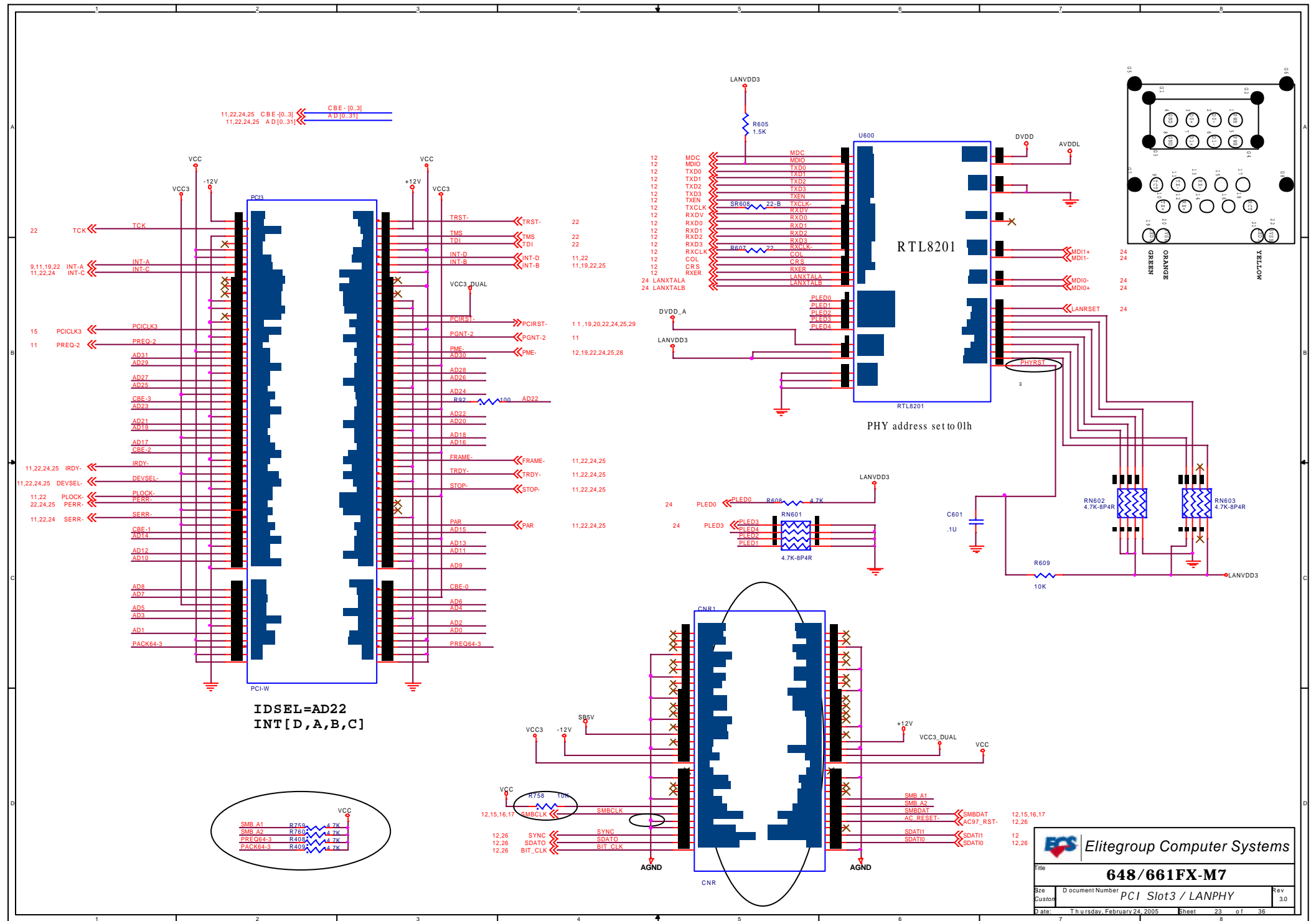


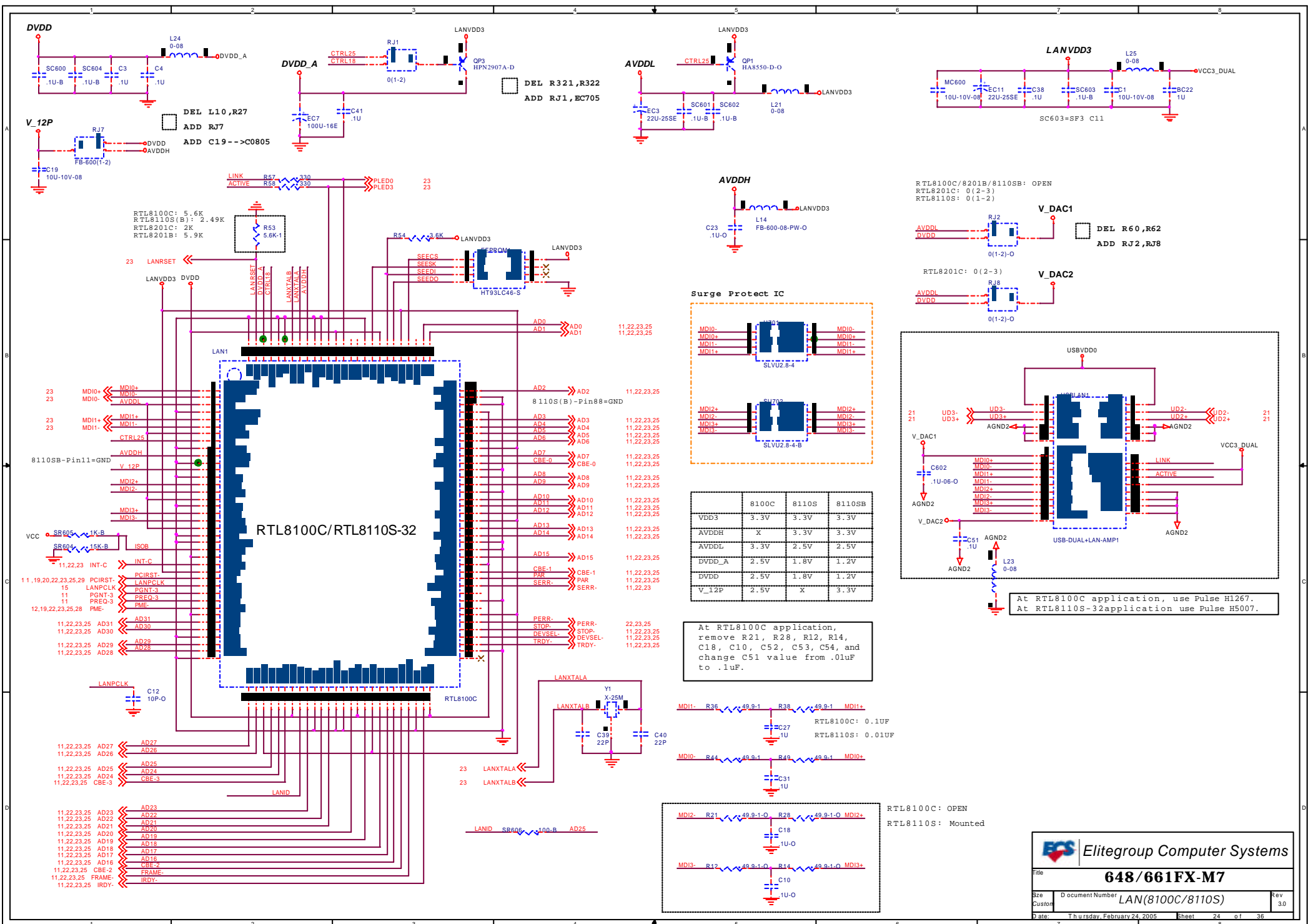
IDSEL=AD21  
INT[C,D,A,B]



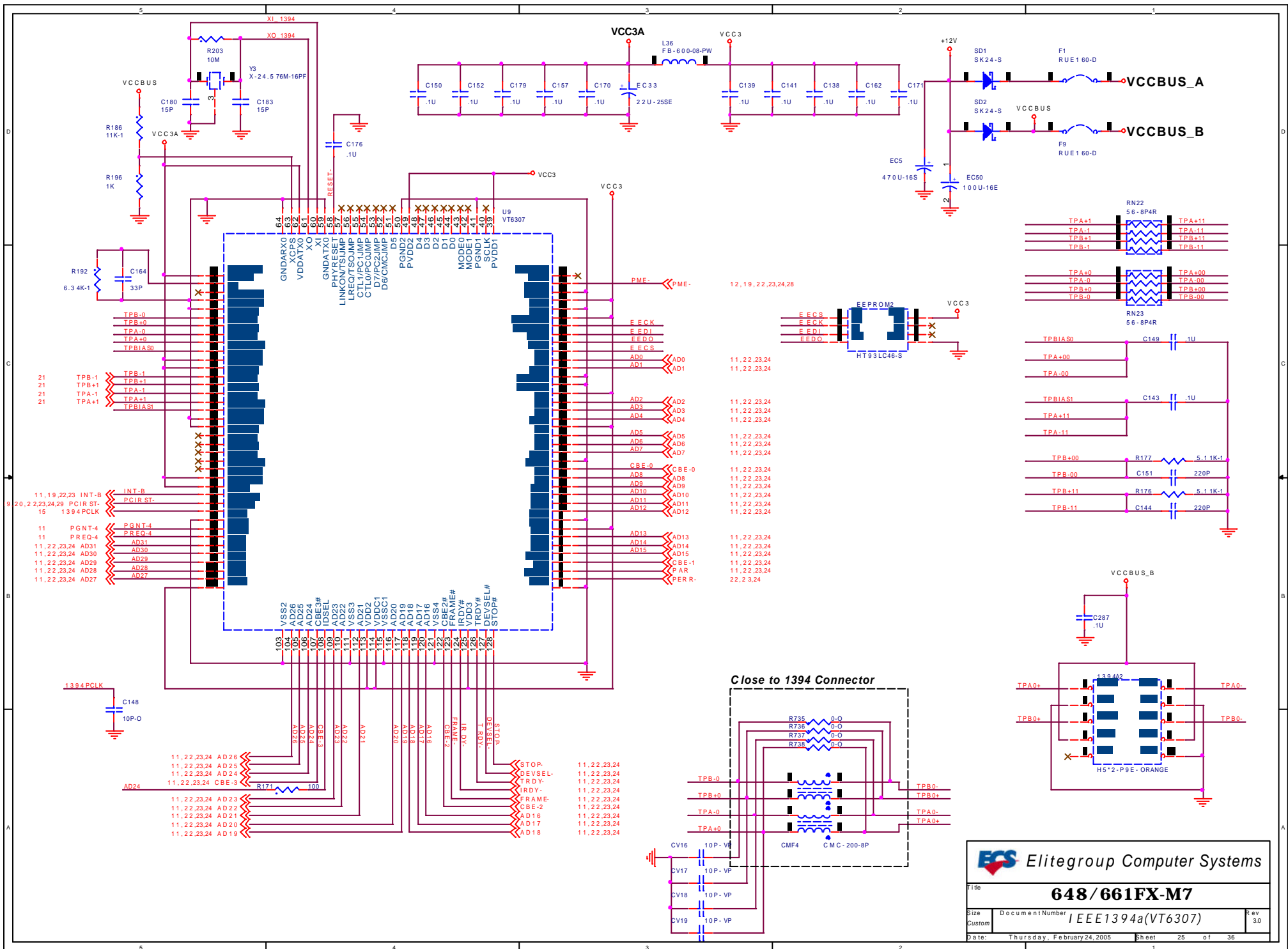
每個 PCI 插槽 pin A33  
各放一顆

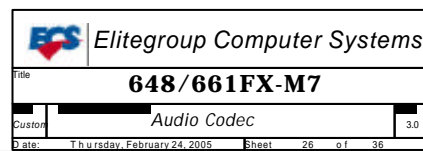


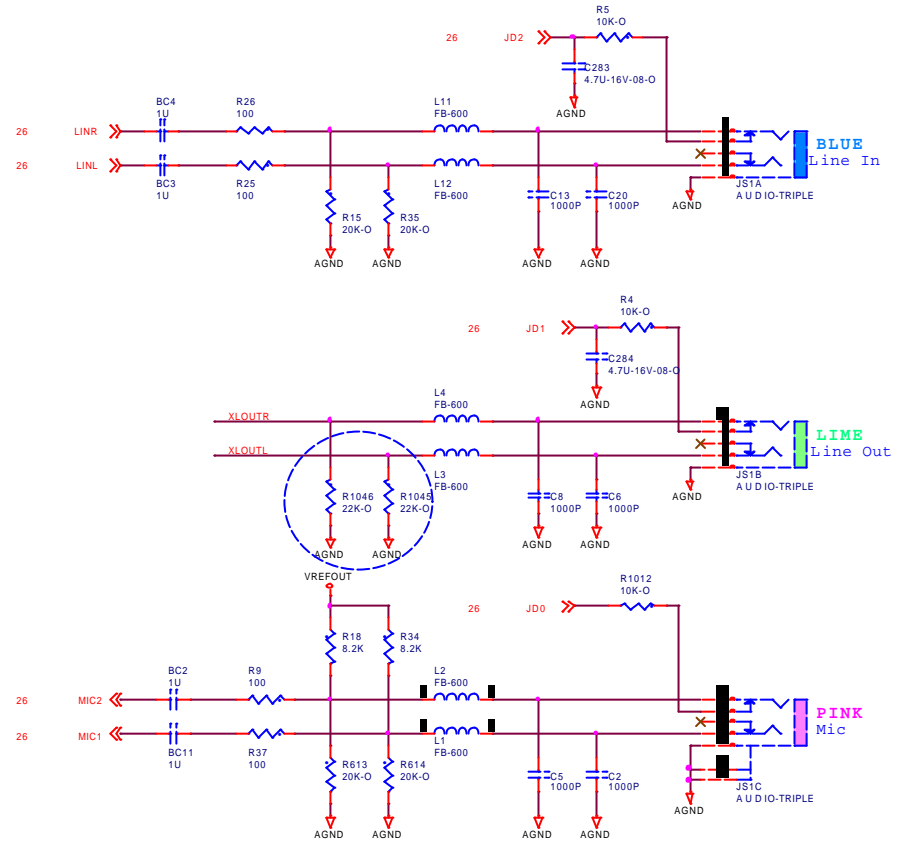
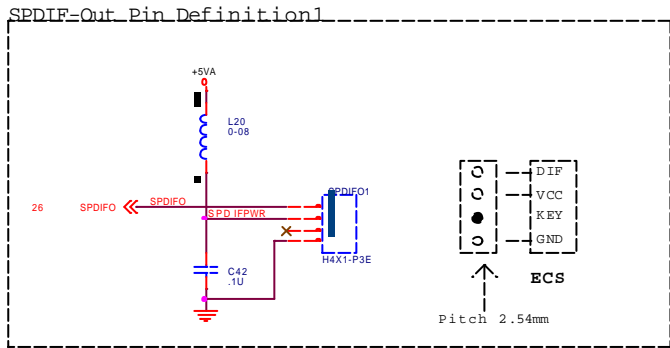
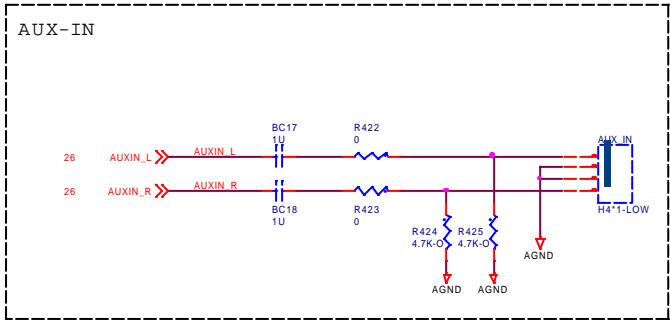
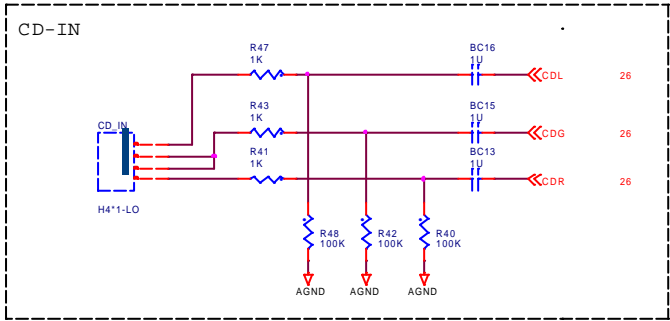
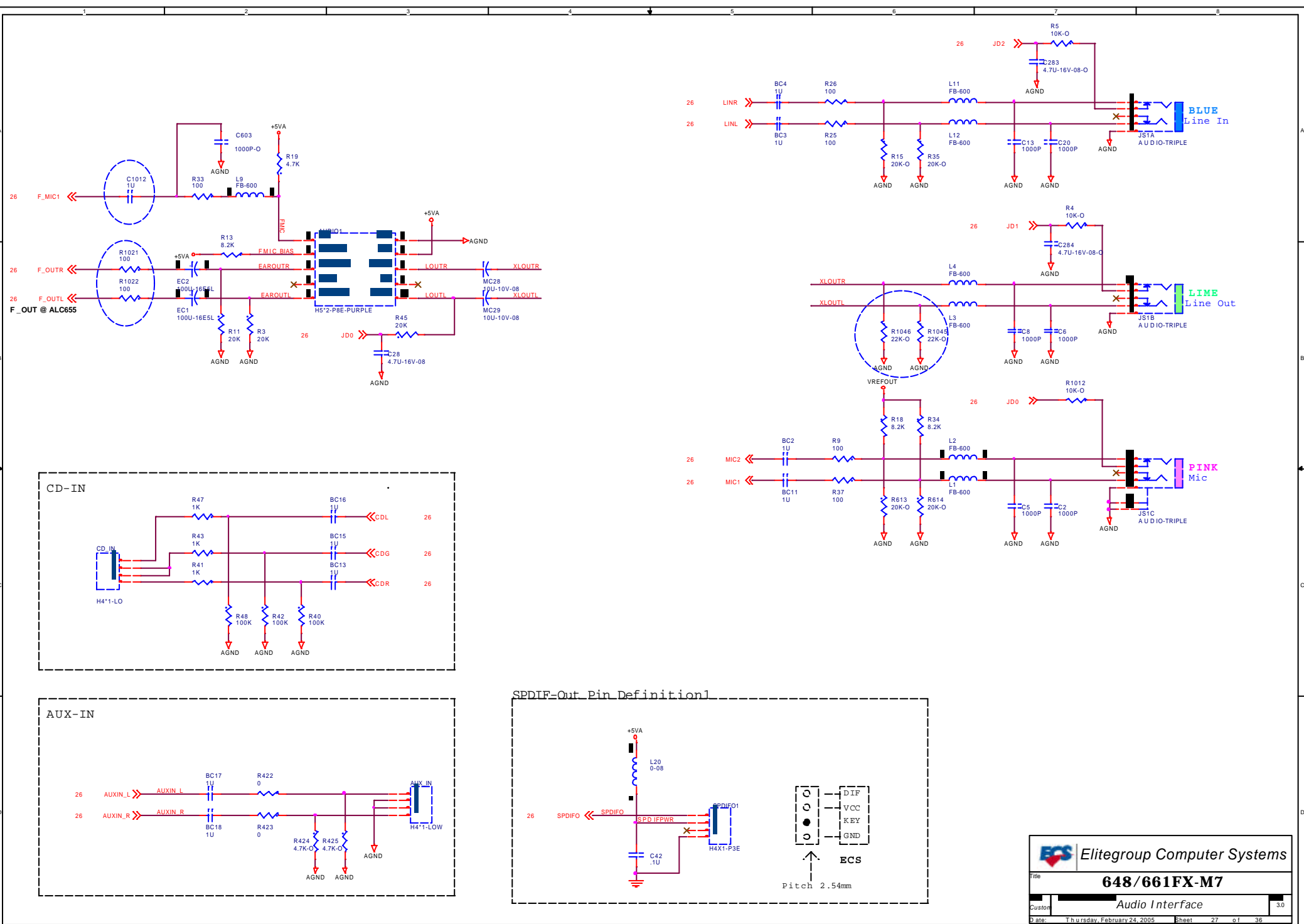


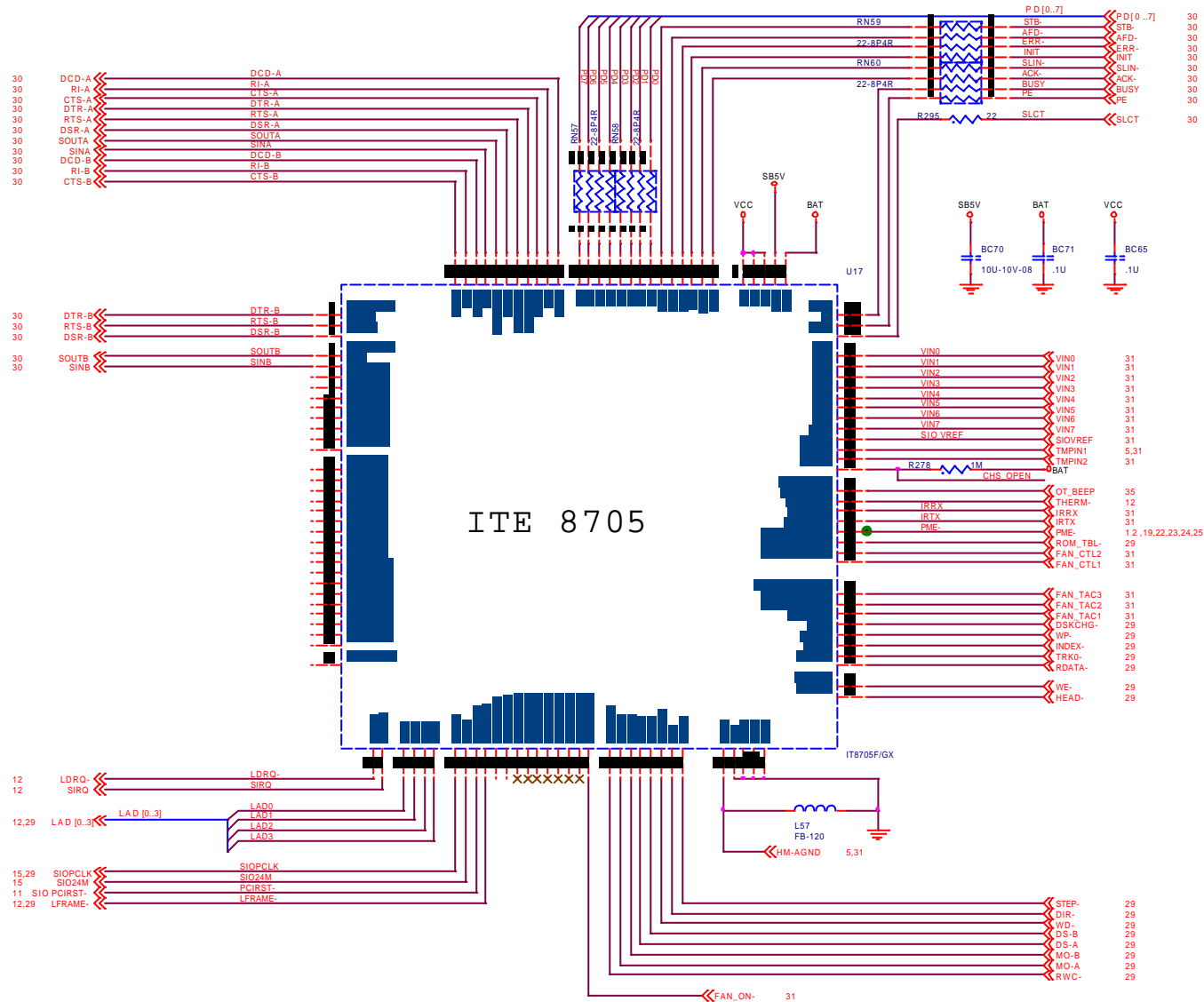




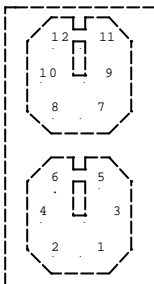








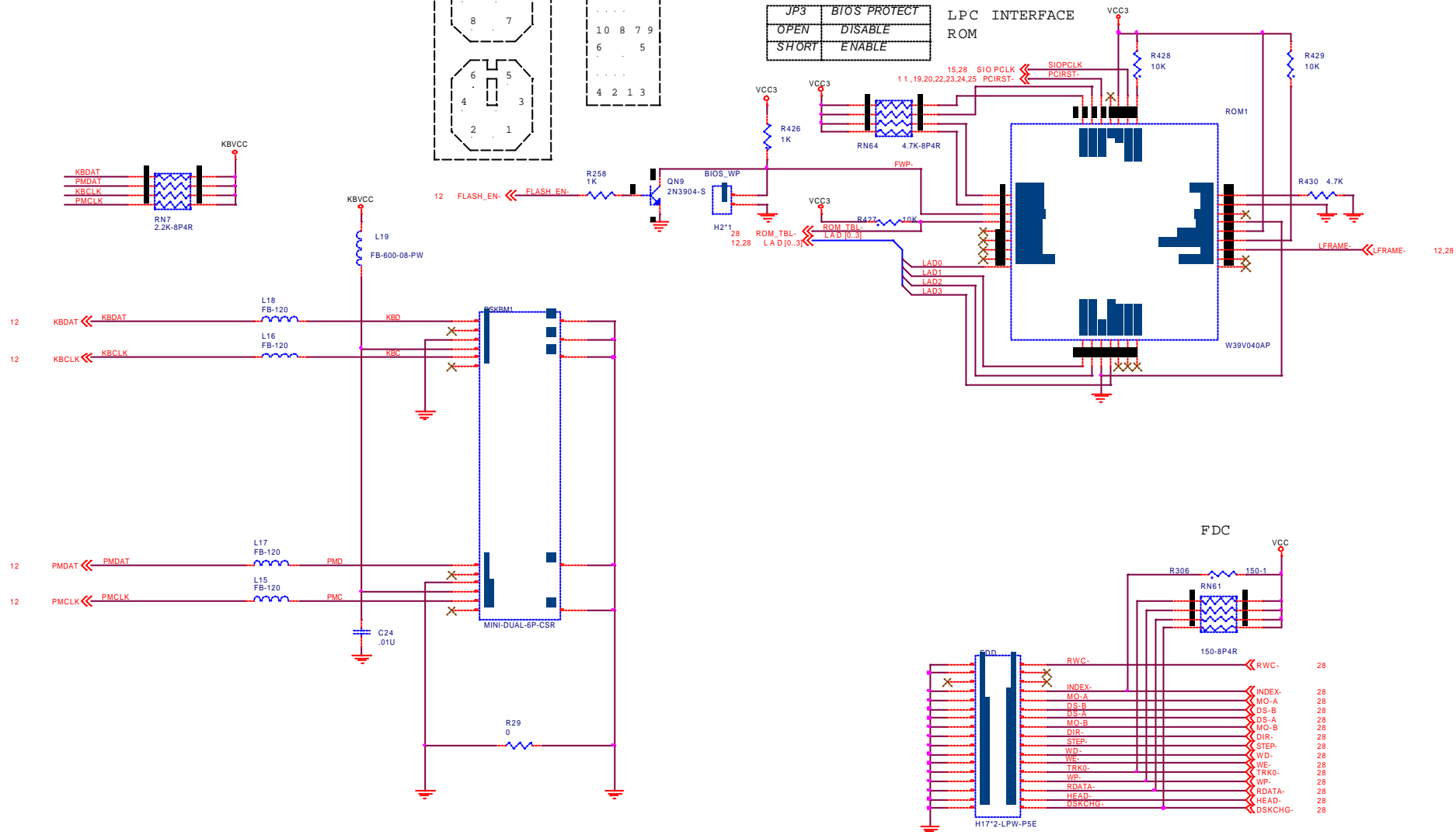
CONNECTOR VIEW



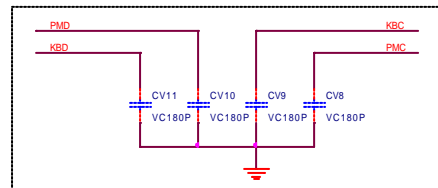
TOP VIEW



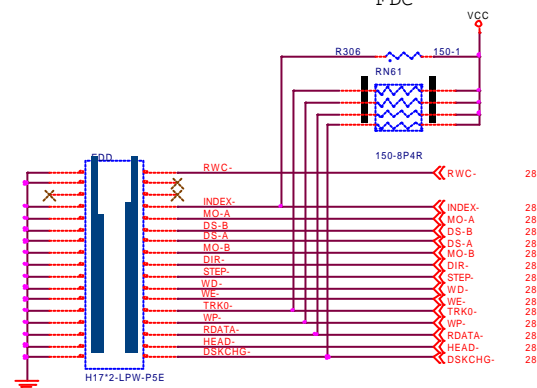
JP3	BIOS PROTECT
OPEN	DISABLE
SHORT	ENABLE

LPC INTERFACE  
ROM

PLACE NEAR CONNECTOR



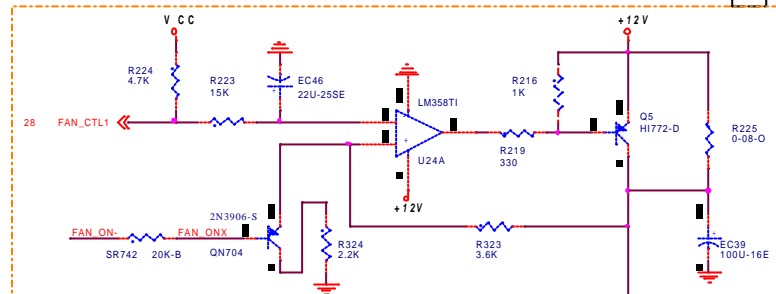
FDC



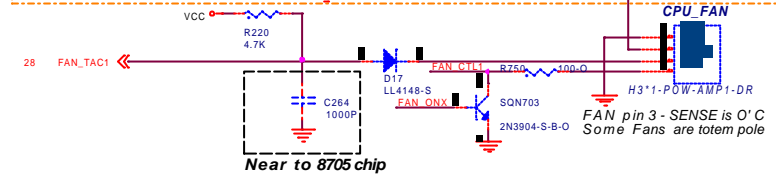


**Layout:**  
Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA.

ADD R223, EC46, R323, R324, R219, R216, R225, Q5, QN704, U24, R415

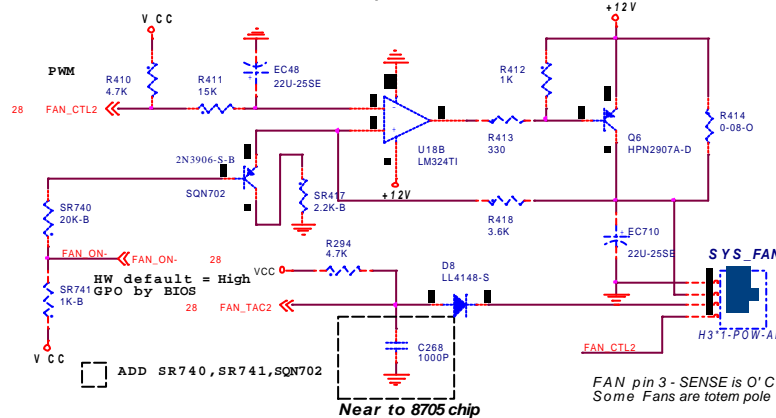


4pin header: SQN703, R750=100ohm, R225=0ohm-0805  
3pin header: R223, EC46, R216, R219, Q5, U24, R415, R324, QN704, R323

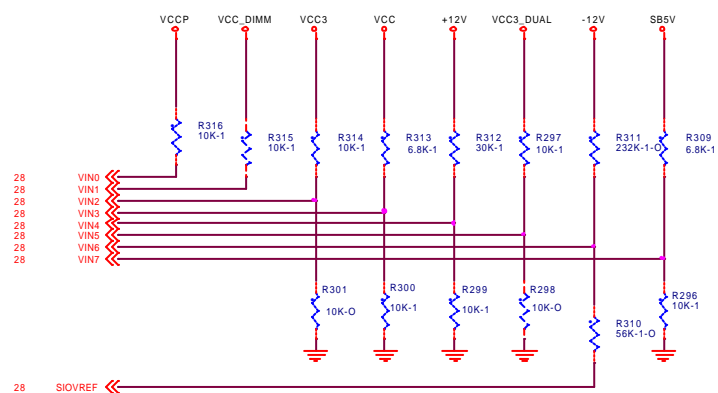


DEL D700

modify SQN702, SR740, SR741, SR742, R417-->SR417

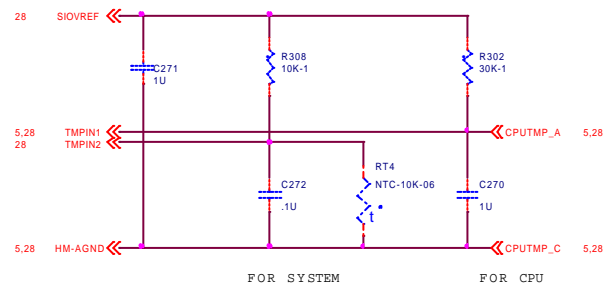


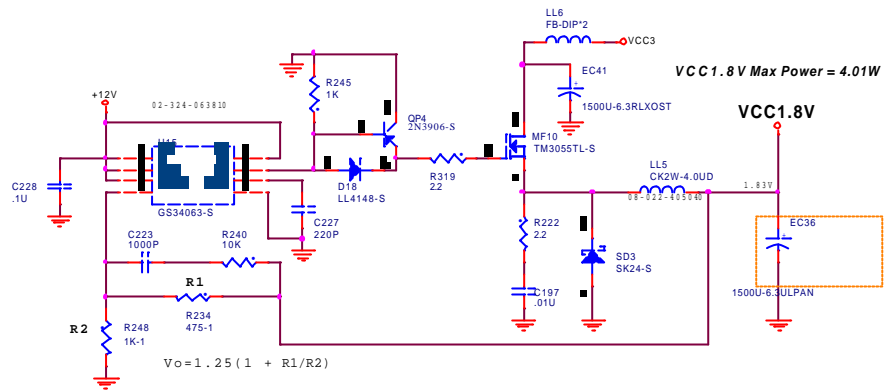
### Voltage Monitor



### Temperature Monitor

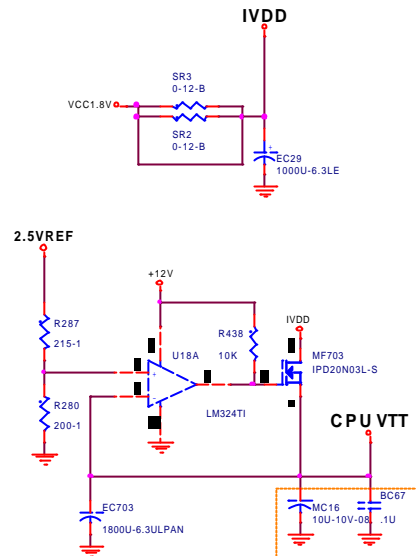
Choosing method of measuring temperature by either thermistor or diode



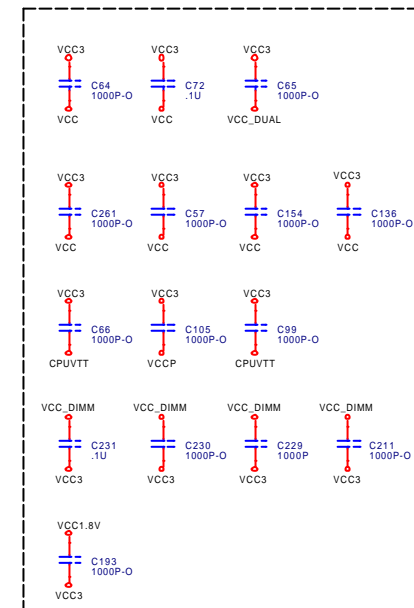
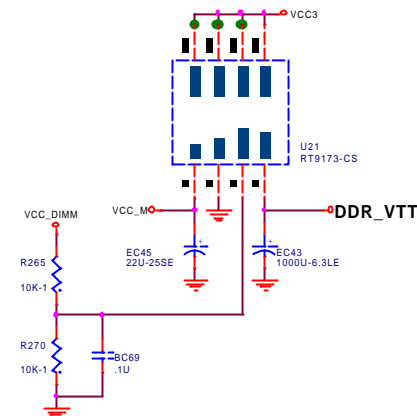


	IVDD	VCC1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator or two regulator

	AUX_IVDD	SB1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator

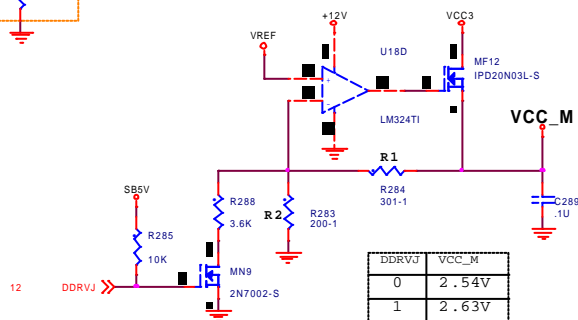
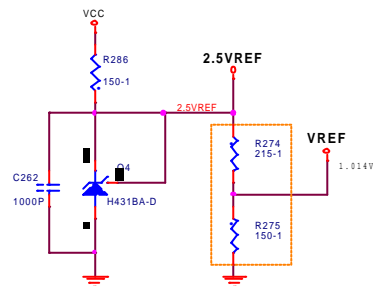
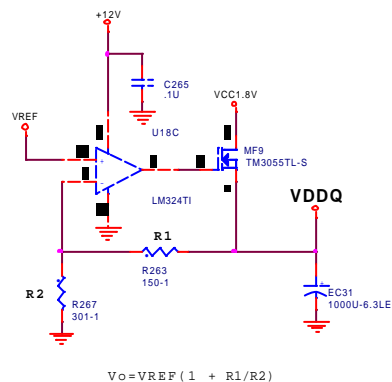


Modify EC703



平均分布在POWER PLAN 和 PLAN 之間

VCC1.5V Max Power = 0.3\*(0.289+2.35)=0.7917W



DDR_VJ	VCC_M
0	2.54V
1	2.63V



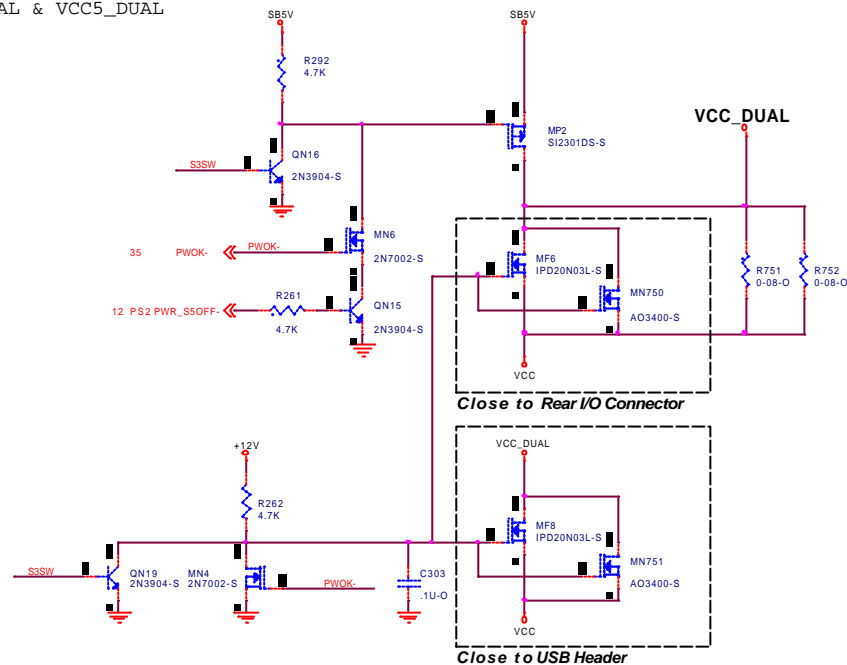
# AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1. IN S0.S1  
THIS CIRCUIT PASSES THE NORMAL POWER

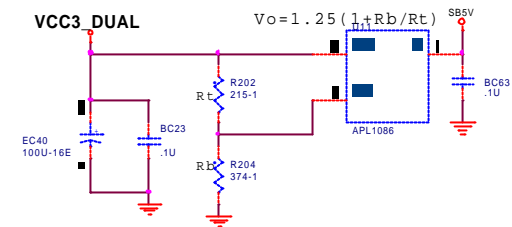
2. IN S3,S4,S5  
THIS CIRCUIT PASSES THE STANDBY POWER

NOTE:  
BECAUSE OF THE MAXIMUM CURRENT FROM  
POWER SUPPLY IS ONLY ABOUT 750-1000mA  
SO IF YOU WANT TO SUPPORT WAKE UP  
FROM S3 BY USB, YOU MUST HAVE A POWER  
SUPPLY WITH LARGER POWER.(ADDITIONAL  
500MA PER USB PORT)

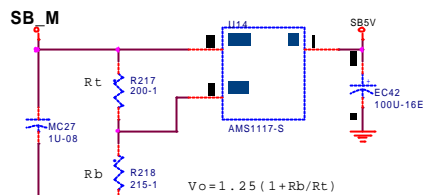
## VCC3\_DUAL & VCC5\_DUAL



## VCC3\_DUAL

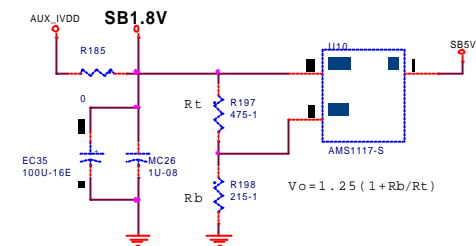


## SB\_M



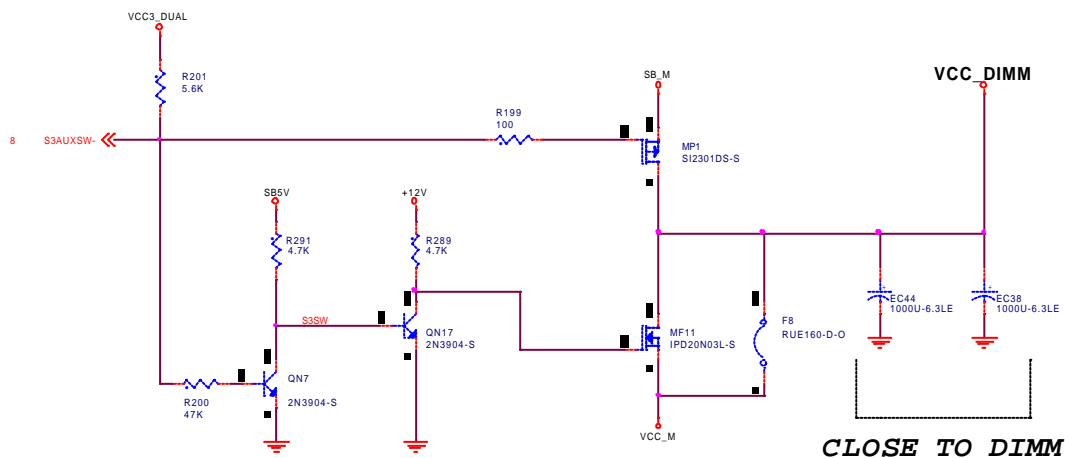
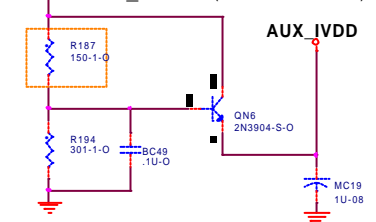
SB1.8V (For SB) 450mA

## SB1.8V

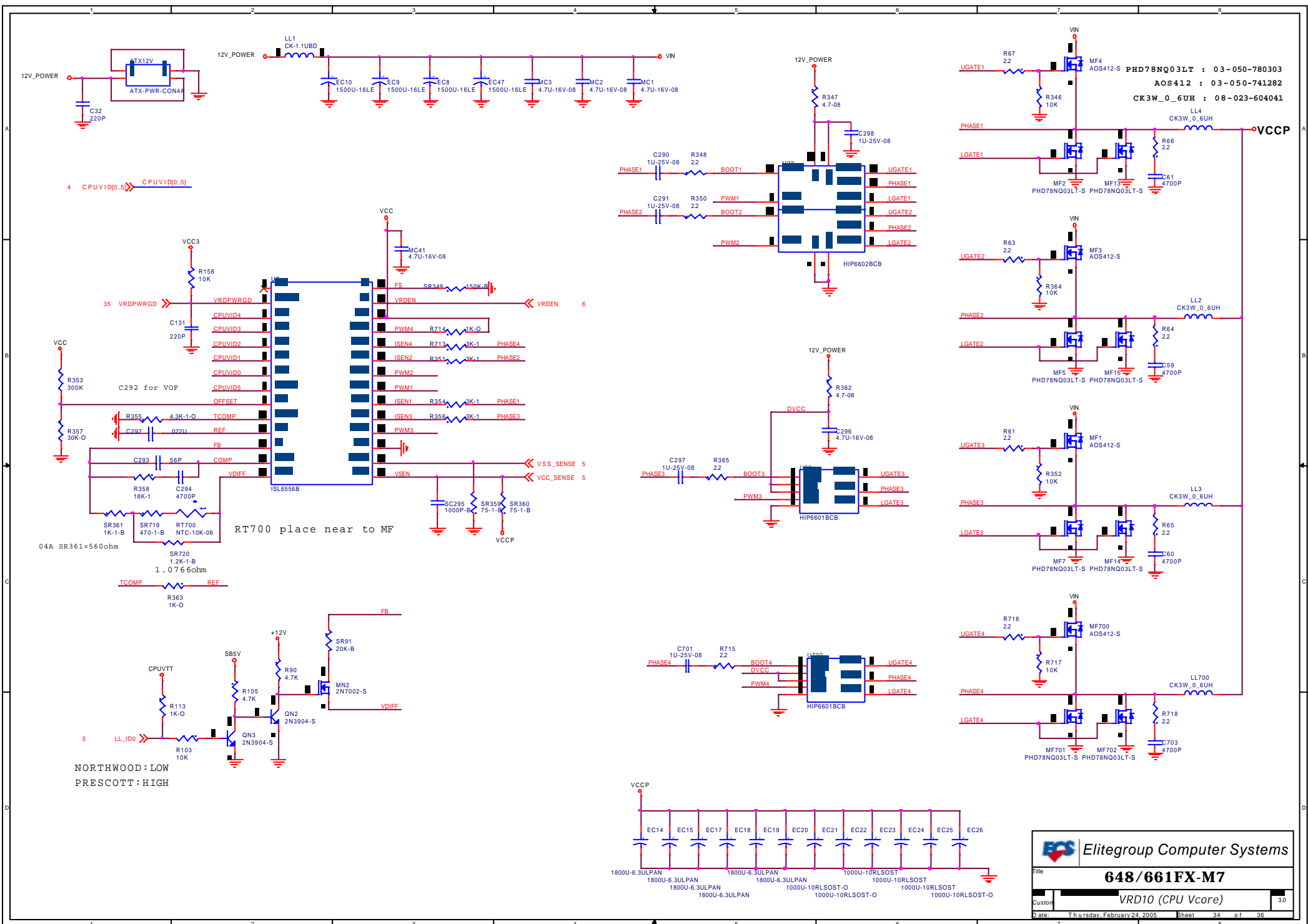


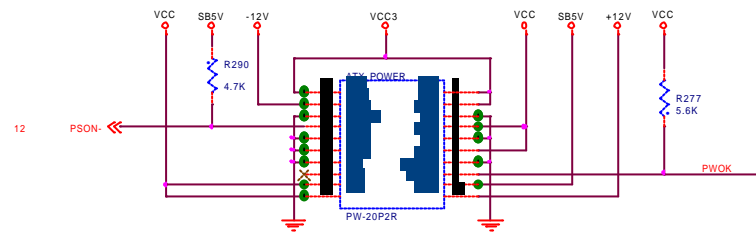
## VCC3\_DUAL

AUX\_IVDD (1.5V For NB) 10mA

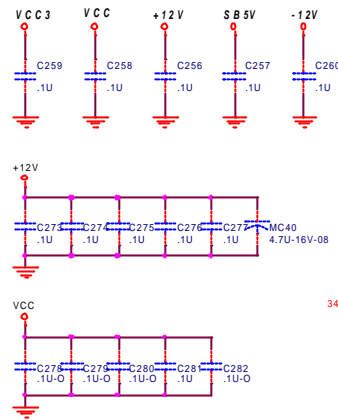


CLOSE TO DIMM

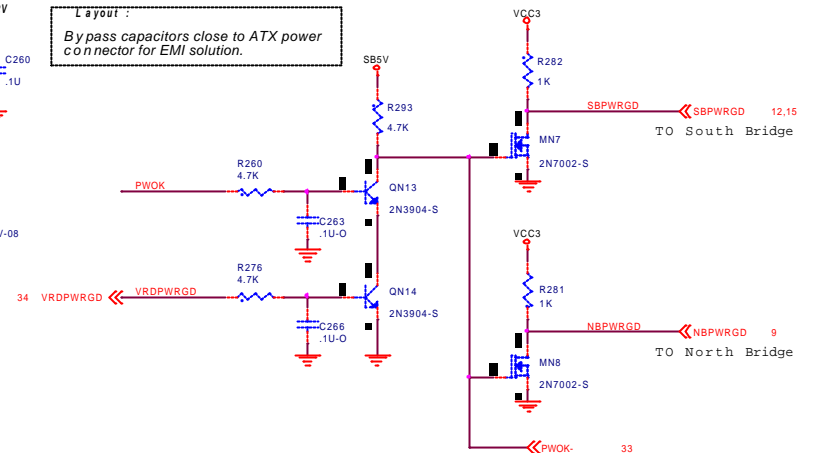




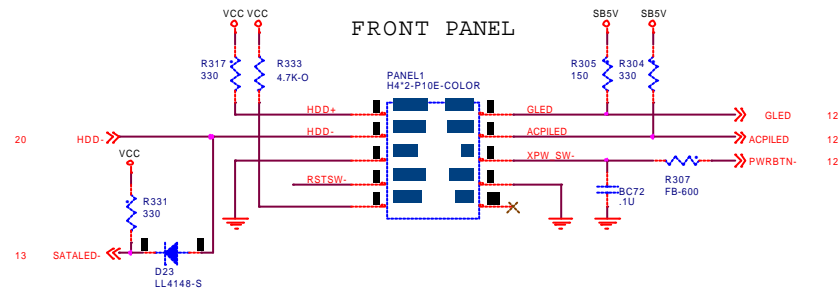
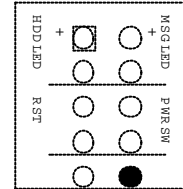
Hardware Reset Circuit



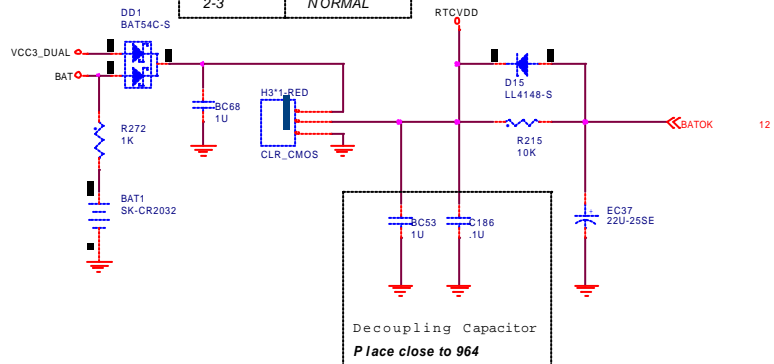
Layout :  
Bypass capacitors close to ATX power connector for EMI solution.



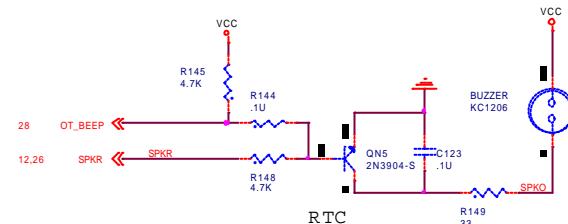
Intel Front Panel



CLR_CMOS	CLEAR CMOS
1-2	CLEAR
2-3	NORMAL



Decoupling Capacitor  
Place close to 964



NOTE!

- 1.The RTCVDD is 3V
  - 2.Decoupling capacitor must be close to 635 RTCVDD pin.
  - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.

## 1. BOM Attention

### (1) South Bridge

Option	SIS964	SIS964L
Components		
U13	964 964142	964L 964162
R241	374 374010	X
R71, R74	33 330000	X
R72, R75	49.9 499010	X
R331	330 330001	X
D23	1N4148 03-021-214890	X
SATA1, SATA2	10-020-007690	X

### (2) On-Board VGA

Option	Support	No Support
Components		
U8	661FX 661141	648FX 648161
L30, L31, L32, L6, L7, L8	FB-120	X
C112, C116, C117, BC35	1U	X
C118, C119	.1U	X
MC36, MC37	10U	X
R136	130 130011	X
R134, R143	33	X
R128, R135	100	X
VGA1	10-717-015010	X
C111, C114, C115	22P	X
R22, R23, R24	75	X
R32, R39	2.2K	X
CV1~7	2P-VP 04-130-220003	X
F2	O	X

### (3) 661FX A1&B1

Option	A1	B1
Components		
U8	A1 661141	B1 964145
R159, SR4	210 210011	169 169011
MN18@ rev1.1	2N3904	0-08(D-S)
MN18@ rev1.2		X
R126	14 140010	10 100010
SR800@ rev1.2	X	0
JPT3@ Standard	Open or (2-3)	(1-2)
JPT3@ Lenovo&TG	(1-2)	(2-3)

### (4) LAN

Option	8100C 10/100 Mbps	8110S 1Gbps	8110SB 1Gbps	8201BL 10/100 Mbps	8201CL 10/100 Mbps
Components					
LAN1	RTL8100C 01-230-100351	RTL8110S 01-230-110350	RTL8110SB	RTL8201BL 02-448-201861	RTL8201CL 02-462-201860
R53	5.6K-1	2.49K-1	2.49K-1	5.9K-1	2K-1
R12, R14, R21, R28	X	49.9	X	X	X
C10, C18	X	0.1u	X	X	X
C52, C53, C54	X	0.01u	X	X	X
C51	0.1u	0.01u	0.01u	X	0.1u
RJ2	X	(1-2) 0 ohm	X	X	(2-3) 0 ohm
R604	X	X	X	X	0 ohm
C601	X	X	X	X	0.1u
L14/ C23	X	0 ohm/0.1u	0 ohm/0.1u	X	X
RJ7/ C19	(1-2)FB-600 /10u-08	X	(2-3)FB-600 /10u-08	X	X
L21	0 ohm	X	X	0 ohm	0 ohm
QP1	X	HA8550	HA8550	X	X
RJ1	(1-2) 0 ohm	(2-3) 0 ohm	(2-3) 0 ohm	X	X
RJ8	X	X	X	X	(2-3) 0 ohm
QP3	HPN2907A	HA8550	HA8550	X	X
RN601, RN602, RN603	X	X	X	4.7K-8P4R	4.7K-8P4R
C601	X	X	X	0.1u	0.1u
R608/ R609	X	X	X	4.7K/ 10K ohm	4.7K/ 10K ohm
R605	X	X	X	1.5 K ohm	1.5 K ohm
R602, R603, R607	X	X	X	22 ohm	22 ohm
SR600/ SR601/ SR602/ SR603/ SR607/ SR608	X	X	X	22 ohm-B	22 ohm-B
SR606	150 ohm-B	150 ohm-B	150 ohm-B	X	X
SR604/ SR605	15K/ 1K ohm-B	15K/ 1K ohm-B	15K/ 1K ohm-B	X	X
Y600/ R600	X	X	X	Y-25 M/ 0 ohm	Y-25 M/ 0 ohm
C166/ C600	4.7K ohm/ X	4.7K ohm/ X	4.7K ohm/ X	22P	22P
R190/ R191	X / 1K ohm	X / 1K ohm	X / 1K ohm	1K ohm/ X	1K ohm/ X
EEPROM1/ EEPROM3	0 / X	0 / X	0 / X	X / 0	X / 0
R54/ R610	3.6K ohm/ X	3.6K ohm/ X	3.6K ohm/ X	X / 4.7K ohm	X / 4.7K ohm

## 2. GPIO Function

GPIO	Status	0	1	Jumper
GPIO5	* RESERVED	RESERVED	RESERVED	JP4
GPIO6	* RESERVED	RESERVED	RESERVED	JP5
GPIO7	* LAN Selection	LANPHY	PCILAN	N/A
GPIO9	USB, PS/2 S4/S5 Wake Up	Disable	Enable	N/A
GPIO10	DDR Voltage	2.54V	2.63V	N/A
GPIO11	* WHQL	No Support	Support	JPT3
GPIO13	Flash Write Protect	Un-Protect	Protect	

(1) "\*" means that the function is selective and ECS may make changes at any time, without notice in this page.

(2) Jumper Setting (Header 3\*1):

1: (1-2)

0: (2-3)

(3) Please see Page.12 for more detail jumper function.

JPT3	1-2	2-3
GPIO11	1	0
HP	Clear CMOS	Normal
TRIGEM	Suspen Mode	S1 & S3

JPT4	1-2	2-3
GPIO5	1	0
HP	Clear Password	Normal
TRIGEM	BIOS Logo	TG

